GMM VDE/VDI-GESELLSCHAFT MIKROELEKTRONIK, MIKRO- UND FEINWERKTECHNIK

Program and Invitation

ICPT

International Conference on Planarization/CMP Technology

October 25 – 27, 2007
Hilton Hotel, Dresden, Germany

www.icpt2007.com

in cooperation with:
German CMP User Group
Japanese Planarization and CMP Technical Committee (JSPE)
Korea CMP User Group (KCMPUG)
Northern California Chapter AVS (NCCAVS) CMPUG
Taiwan CMP User Group (CMPUGTW)

Fraunhofer Institut Siliziumtechnologie

VDI

VDE

Conference Objective

Over the last 15 years, Chemical Mechanical Polishing (CMP) has developed into one of the key technologies in the ULSI fabrication process. It can be viewed as an enabling technology for manufacturing state-of-the-art microprocessors, high-density memories and other advanced microelectronic circuits. Without CMP, accurate printing of nanometer chip structures is impossible. CMP has helped to introduce multilevel interconnection and the employment of copper metallization. Emerging CMP applications include MEMS and nanotechnology, but advancements in CMP also stimulate related areas like wafer polishing and production of optical surfaces. In order to keep pace with future ULSI developments, improved Chemical Mechanical Polishing processes have to be available for FEOL and BEOL applications. For reasons of productivity enhancement, tool reliability improvements, cost reductions, process automation and advanced process control are required. Finally, new fields of applications for CMP, which certainly exist plentiful, have to be discovered and developed.

Upon several requests towards increased co-operation of the local CMP users groups from Germany, Japan, Korea, Taiwan, and the United States of America, the idea of a joint international CMP conference emerged in 2005. Following successful conferences in Tokyo, Japan (PacRim-CMP 2004), Seoul, Korea (PacRim-CMP 2005) and Foster City, California, USA (ICPT 2006), the International Conference on Planarization/CMP Technology ICPT 2007 in Dresden, Germany, is organized by the German CMP User Group within the German VDE/VDI-Society Microelectronics, Micro- and Precision Engineering. The mission of this conference is the provision of a forum for the worldwide CMP community for exchange and discussion on a high scientific level in order to support and advance the developments of this highly important field of semiconductor manufacturing.

Dr. Gerfried Zwicker
Fraunhofer Institute for Silicon Technology (ISIT)
Conference Chairman

List of Contents

Page

Organizing Committee 4

Organizer 5

Program Overview 6

- Thursday, October 25, 2007 6
- Poster Session 1 10
- Friday, October 26, 2007 14
- Poster Session 2 18
- Saturday, October 27, 2007 22

Conference Information 23

- Conference Hours 23
- Registration Hours 23
- Exhibition 23

Information for Authors 23

General Information 24

- ICPT Secretariat 24
- Conference Fees 24
- Conference Registration 24
- Online Registration 25
- Payment 25
- Cancellation 25
- Proceedings 25
- Venue 26
- Hotel Reservation 26/27
- Busshuttle to the Conference Hotel 27
- Insurance 27
- Passport and Visa Requirements 28
- Transport 28

List of Exhibitors 29

List of Sponsors 32

Organizing Committee

International Executive Committee:

Keiichi Kimura, Kyushu Institute of Technology, Japan
Jin-Goo Park, Hanyang University, Korea
Daniel Shen, BASF, Taiwan
Halbert Tam, JSR Micro Inc., USA
Gerfried Zwicker, Fraunhofer Institute for Silicon Technology, Germany

International Program Committee:

S.V. Babu, Clarkson University, USA
S. Balakumar, Institute of Microelectronics, Singapore
Chao-Chang Chen, University of Science and Technology, Taiwan
Toshiro Doi, Saitama University, Japan
David Dornfeld, University of Berkeley, USA
Wei Yung Hsu, Applied Materials, USA
Masaharu Kinoshita, Nitta Haas Inc., Japan
Seiichi Kondo, Selete, Japan
Scott Lawing, Rohm & Haas, USA
Inkyung Lee, Cheil Industries Inc., Korea
Hitoshi Morinaga, Tohoku University, Japan
Chan-Kwon Oh, Doosan D&D, Korea
Hyung-Soon Park, Hynix, Korea
Maria Peterson, JSR Micro, USA
Mike Pevny, 3M, USA
Ara Philipossian, University of Arizona, USA
Haedo Jeong Pusan, National University, Korea
Manabu Tsujimura, Ebara, Japan
Bo-Un Yoon, Samsung Electronics, Korea

International Advisory Board:

Geun Min Choi, Hynix, Korea
Laertis Economikos, IBM, USA
Chang-Ki Hong, Samsung, Korea
Markus Keil, AMD, Germany
Sang-Yong Kim, Dongbu Electronics, Korea
Motoshu Miyajima, Fujitsu, Japan
Mansour Moinpour, Intel, USA
Yongsik Moon, AMD, USA
Stan Smith, TI, USA
Dorit Wecker, Infineon Technologies, Germany
Yohei Yamada, Hitachi, Japan

Local Organization and Program Committee:

Johann W. Bartha, Dresden Technical University, Germany
Katrin Blum, IHP, Germany
Knut Gottfried, Fraunhofer IZM, Germany
Karl Hensen, BASF AG, Germany
Michael Kroell, Degussa, Germany
Martin Kulawski, VTT, Finland
Georg Moersch, Peter Wolters AG, Germany
Uwe Stoeckgen, AMD, Germany
Peter Thieme, Qimonda AG, Germany
Dorit Wecker, Infineon Technologies AG, Germany
Gerfried Zwicker, Conference Chairman, Fraunhofer Institute for Silicon Technology, Germany

Organizer

VDE/VDI-Society Microelectronics, Micro- and Precision Engineering (GMM)
Dr. Ronald Schnabel
Stresemannallee 15
D-60596 Frankfurt am Main
Germany
Phone: ++49-69-6308-330
Fax: ++49-69-6308-9828
E-Mail: gmm@vde.com

PROGRAM OVERVIEW

Wednesday, October 24, 2007

17:00 h - 19:00 h **Registration**

19:00 h **Set up for Technical exhibition**

Thursday, October 25, 2007

07:30 **Registration**

09:00 **Welcome to Conference**
G. Zwicker, Fraunhofer Institute for Silicon Technology, Itzehoe, Germany

09:05 **Challenges and opportunities of semiconductor manufacturing between research and volume production**
H.Deppe, AMD Dresden, Germany

Session 1: CMP Fundamentals 1

Session Chairs:
S.V. Babu, Clarkson University;
Peter Thieme, Qimonda

09:30 **CMP Modeling as a Part of Design for Manufacturing (Invited)**
S. Tripathi, A. Monvoisin, D. Dornfeld, F.M. Doyle;
University of California at Berkeley, CA, USA

09:55 **Pad Surface Analysis and Conditioning Effects: Implications on Process Design, Break-in Response and Next Generation Pad and Conditioning Platforms**
S. Lawing, C. Juras;
Rohm and Haas Electronic Materials, Phoenix, AZ, USA

10:15 **Tribological, Kinetic, Thermal and Flow Characteristics of Retaining Rings in STI CMP**
X. Wie[1], A. Philipossian[1,2], Y. Zhuang[1,2], Y. Sampurno[1], F. Sudargho[1,2], C. Wargo[3], L. Borucki[2];
[1]University of Arizona, Tucson, AZ, USA;
[2]Araca Inc, Tucson, AZ, USA;
[3]Entegris Corp., Billerica, MA, USA

10:35 **In-Situ Investigation of Wafer-Slurry-Pad Interactions during CMP**
C. Gray[1], A. Mueller[1], J. Vlahakis[1], V.P. Manno[1], C. Rogers[1], R. White[1], S. Anjur[2], M. Moinpour[3],
[1]Tufts University, Medford, MA, USA;
[2]Cabot Microelectronics Corp., Aurora, IL, USA;
[3]Intel Corp., Santa Clara, CA, USA

10:55 **Coffee Break**
Poster Session 1: CMP of Poly-Si, Dielectrics and Metals, Fundamentals
(all Posters in Poster Session 1 are listed on page 10)

Session 2: Metal CMP 1

Session Chairs:
Yohei Yamada, Hitachi;
Karl Hensen, BASF

11:55 **CMP of a Ru Based Layer in an Advanced Cu Low-k Stack (Invited)**
J. Vaes, F. Sinapi, J. L. Hernandez;
IMEC, Heverlee, Belgium

12:20 **Integrated Profile Control from ECP to CMP**
U. Stöckgen, S. Wehner, A. Preuße, J. Heinrich, J. Groschopf; AMD Fab36, Dresden, Germany

12:40 **A Systematic Study on the Impact of Polymer Additives in Bulk Copper Slurry on Copper CMP**
H. Chou, W.L. Kim, J.I. Noh, I. Lee;
Samsung Cheil Industries, Korea

13:00 **Full Sequence eCMP for Advanced Low Stress Copper Planarization**
J. Groschopf[1], K. Steffen[1], R. Donohue[2], P. Lo-Menzo[2], R. Seidel[1], M. Grillberger[1], H. Gu[3], Y. Hu[3], Y. Wang[3], W.-Y. Hsu[3];
[1]AMD Fab36, Dresden, Germany;
[2]Applied Materials, Dresden, Germany;
[3]Applied Materials, Sunnyvale, CA, USA

13:20 **Lunch / Coffee**
Poster Session 1: CMP of Poly-Si, Dielectrics and Metals, Fundamentals
(all Posters in Poster Session 1 are listed on page 10

Session 3: Wafers and New Materials

Session Chairs:
Haedo Jeong, Pusan National University;
Knut Gottfried, Fraunhofer IZM Chemnitz

14:50 **Challenges in CMP of New Materials from Carbon Nanotubes to Moisture Sensitive Surfaces (Invited)**
Y. Li, Clarkson University; Potsdam, NY, USA

15:15 **Influence of the Wafer Shape on Polishing Performance for 300 mm Prime Wafer Polishing**
M. Langenkamp, J. Kanzow, G. Mörsch; Peter Wolters AG, Rendsburg, Germany

15:35 **Application of CMP to the Cladding Layer of MRAM**
S.-H. Wang, D.-Y. Shu, K.-C. Lin, C.-T. Yen, M.-J. Tsai; Industrial Technology Research Institute, Hsinchu, Taiwan

15:55 **TaN Formation by CMP for Cross-Spacered Phase Change Memory**
K.-C. Lin, C.-W. Chen, S.-H. Wang, D.-Y. Shu, M.-J. Tsai, M.-J, Kao; Industrial Technology Research Institute, Hsinchu, Taiwan

16:15 **Coffee Break**
Poster Session 1: CMP of Poly-Si, Dielectrics and Metals, Fundamentals
(all Posters in Poster Session 1 are listed on page 10)

Session 4: Poly-Si & Dielectric CMP 1

Session Chairs:
Mansour Moinpour, Intel;
Dorit Wecker, Infineon Technologies

17:15 **Planarization of the Poly-Si Gate for Non Volatile Memories (Invited)**
L. Baud[1], L. Canevari[2], C. Romanelli[2], G. Spinolo[2], M. Rivoire[3];
[1]CEA-LETI, Grenoble, France;
[2]ST Microelectronics, Agrate Brianza, Italy;
[3]ST Microelectronics, Crolles, France

17:40 **Effect of Polish Stopper Film in STI-CMP for 45nm Node Devices and Beyond**
T. Watanabe[1], S. Shibata[2], N. Idani[1], M. Kase[1], M. Miyajima[1];
[1]Fujitsu Ltd., Tokyo, Japan;
[2]Fujitsu Laboratories Ltd., Tokyo, Japan

18:00 **Influence of STI Trench Fill and Dummy Design on CMP Behavior**
P. Ong[1], K. Devriendt[1], A. Redolfi[1], Y. Okuno[2], J.L. Hernandez[1],
[1]IMEC, Leuven, Belgium;
[2]Matsushita, Japan

18:20 **Defectivity Improvement for Fixed Abrasive Based STI CMP in Advanced Logic Technology**
B. Reinhold[1], J. J. Gagliardi[2], S. Endle[2],
[1]AMD Fab36, Dresden, Germany;
[2]3M Electronics Markets Materials Division, St. Paul, MN, USA

18:40 **End of Sessions (Day 1)**

19:30 **Conference Dinner**
at the Pulvertum
An der Frauenkirche 12, 01067 Dresden

Thursday, October 25, 2007
Poster Session 1: CMP of Poly-Si, Dielectrics and Metals, Fundamentals

About the Wafer/Pad Interaction, Pad Surface Dynamics, Asperities, Defectivity, Pad Conditioning and Other CMP Fundamental Constituents
Y. Gotkis, KLA-Tencor Corp., San Jose, CA, USA

Insitu Studies of Copper CMP with Arginine and Peroxide Based Slurries
Y. Nagendra Prasad, S. Ramanathan; Indian Institute of Technology-Madras, Chennai, India

Bench Top Dual Mode eCMP Polisher with Multi Sensing Metrology
N. Gitis, V. Khosla, M. Vinogradov; CETR, Campbell, CA, USA

Microscopic and Macroscopic Friction in CMP
L. Borucki[1], Y. Zhuang[1,2], T. Sun[2], A. Philipossian[1,2];
[1]Araca Inc., Tuscon, AZ, USA;
[2]University of Arizona, Tucson, AZ, USA

Charakterization of Residual Stress Change of Dielectrics in W-CMP Process Using Finite Element Method Analysis
A. Fukuda[1], Y. Mochizuki[1], H. Hiyama[1], M. Tsujimura[2],
[1]Ebara Research Co., Ltd., Kanagawa, Japan;
[2]Ebara Corp., Kanagawa, Japan

The Study of CVD Diamond Conditioner
N. Rikita, R. Matsuki, H. Kobayashi, M. Nakamura, K. Chida; Mitsubishi Materials Corp., Saitama, Japan

Voltage-Activated Electrochemical Reactions of Copper for Electrochemical Mechanical Polishing Applications
Y.-J. Seo[1], S.-I. Lee[1], S.-W. Park[2], S.-J Han[2], Y.-K. Lee[2], W.-S. Lee[2];
[1]Daebul University, South Korea;
[2]Chosun University, South Korea

Effect of Pad Hole on ECMP Process
S. Jeong[1], H. Lee[1], J. Park[1], H. Jeong[1], H. Kim[2];
[1]Pusan National University, Busan, Korea;
[2]Korea Institute of Industrial Technology, Busan, Korea

Next Generation Barrier CMP Technology for 45nm and Beyond
C. Ye, H. Li; Rohm and Haas Electronic Materials CMP Technology, Newark, DE, USA

Poly-CMP Integration for Sub 90 nm Self-aligned Floating Gate Flash Memories
M. Mariani, C. Romanelli, L. Canevari; ST Microelectronics, Agrate Brianza, Italy

Pre-polishing Transient Effects Investigation for Chemical Mechanical Planarization Processes
A. Filippini[1], C. Patini[2];
[1]ST Microelectronics, Agrate Brianza, Italy;
[2]Applied Materials, Caponago, Italy

Effect of Ceria Size and Concentration in Shallow Trench Isolation (STI) Chemical Mechanical Polishing (CMP)
S. Pandija[1], G. Crinière[2], C. Ceintrey[2], S.V. Babu[1];
[1]Clarkson Unversity, Potsdam, NY, USA;
[2]Rhodia Electronics and Catalysis, France

Next Generation Chemical Mechanical Planarization Slurries for Polishing Silicon on Advanced Devices
M. L. White, C. W. Nam, F. Batllo, A. Walters; Cabot Microelectronics Corp., Aurora, IL, USA

Control of Flatness for Chemical Mechanical Planarization
A. Nutsch, L. Pfitzner; Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany

A Study on Delamination of Low-k Dielectrics During Cu-low k CMP
J.-H. Han[1], D.-H. Chung[1], B.-R. Park[1], J.-B. Yim[1], T.-H. Ahn[1], J.-G. Park[2];
[1]Samsung Electronics Ltd., Kyunggi-Do, Korea;
[2]Hanyang University, Ansan, Korea

Effect of Slurry pH on Poly Silicon CMP
Y.-J. Kang[1], B.-K. Kang[1], J.-G. Park[1], Y.-K. Hong[2], S.-Y. Han[2], S.-K. Yun[2], B.-U. Yoon[2], C.-K. Hong[2],
[1]Hanyang University, Ansan, Korea;
[2]Samsung Electronics, Hwasung, Korea

Development of Post Ru CMP Cleaning Solutions

I.-K. Kim, B.-G. Cho, T.-G. Kim, J.-G. Park; Hanyang University, Ansan, Korea

Pad Roughness Effects on Removal Rate and Selectivity in a STI Ceria CMP Process

F. C. Meyer[1], C.-H. Kuo[2], C. Rudolph[1], P. Faustmann[1];
[1]Qimonda, Dresden, Germany;
[2]Nanya Technolgy Corp., Taoyuan, Taiwan

CMP Issues Arising from Novel Materials and Concepts in the BEOL of Advanced Microelectronic Devices

K. Gottfried[1], I. Schubert[1], K. Schulze[2], S. Schulz[2], T. Gessner[1,2]; [1]Fraunhofer-Institute Reliabilty and Micro-Integration, Chemnitz, Germany;
[2]Technical University Chemnitz, Germany

Impact of Ceria Properties and CMP Parameters on STI CMP Performance

J. De Messemaeker[1], F. Sinapi[2], P. Ong[2], S. Put[1], D. Nelis[1], J. van den Bosch[1], Y. Strauven[1], P. Lippens[1], K. Devriendt[2];
[1]Umicore R&D, Olen, Belgium;
[2]IMEC, Leuven, Belgium

Major Influences of Shaping and Profiling of Cu ECP and CMP on Feature Level for Process Stabilizing

G. Marxsen, M. Nopper, T. Ortleb, M. Lehr, T. Merbeth, T. Roessler; AMD, Dresden, Germany

Advanced W-CMP Slurry for High Planarity

R. Tanaka, H. Nojo, K. Yoshida, A. Isobe; Nitta Haas Inc., Kyotanabe-Shi, Japan

New Polish Chemistry and Process for Improved Fixed Abrasive CMP Performance

G. Menk, R. Marks, G. Leung, A. Iyer, J. Diao, Y. Zhou, C. Lee; Applied Materials, Sunnyvale, Ca, USA

Improvement of Uniformity Post Oxide CMP by Optimization of Pre Processes

T. Schest, J. Plagmann, S. Willkofer; Infineon Technologies, Regensburg, Germany

Novel Chemicals and Mechanisms that Control Dishing and Overpolish Window Independent of Corrosion Inhibitor Effects

S. Shrauti, B. Palmer, A. Meyers, G. Zhang, A. Zutshi; DuPont Air Products NanoMaterials, Tempe, AZ, USA

Application of the Copper Damascene Process for the Preparation of Electromigration Test Structures

M. Stangl[1], V. Hoffmann[1], K. Wetzig[1], U. Künzelmann[2], J.-W. Bartha[2];
[1]Leibniz-Institute for Solid State and Materials Research (IFW) Dresden;
[2]Dresden University of Technology, Dresden, Germany

Friday, October 26, 2007

08:30 **Morning Welcome**
G. Zwicker, Fraunhofer Institute for Silicon Technology, Itzehoe, Germany

Session 5: Poly-Si & Dielectric CMP 2

Session Chairs:
Jin-Goo Park, Hanyang University;
Georg Moersch, Peter Wolters AG

08:35 **Materials & Metrology Challenges in Planarization and Interconnect Technologies (Invited)**
M. Moinpour; Intel, Santa Clara, CA, USA

09:00 **Integrative Defect Reduction at STI CMP (Invited)**
R. Becker, W. Tittes, A. Boenicke, S. Peters, M. Probst, D. Schulze, S. Cwikla, S. Loesch; Infineon Technologies, Dresden, Germany

09:25 **Novel Slurries for Achieving a Low Silicon Dioxide and High Silicon Nitride Removal During Chemical-Mechanical Planarization**
A. Natarajan, Dandu Veera P.R., S.V. Babu; Clarkson University, Potsdam, NY, USA

09:45 **Applications of Shear Force Spectral Analysis in STI CMP**
Y. Sampurno[1], F. Sudargho[1,2], Y. Zhuang[1,2], T. Ashizawa[3], H. Morishima[3], A. Philipossian[1,2];
[1]University of Arizona, Tucson, AZ, USA;
[2]Araca Inc., Tucson, AZ, USA;
[3]Hitachi Chemical Co., Tokyo, Japan

10:05 **Study of STI CMP Process Control on High Aspect Ratio Gap-fill Topographies by Motor Current EPD**
C.-H. Kuo[1], F. C. Meyer[2], M. Hollatz[2], P. Faustmann[2], K.-W. Chung[1], C.-K. Lin[1];
[1]Nanya Technolgy Corp., Taoyuan, Taiwan;
[2]Qimonda, Dresden, Germany

10:25 **Coffee Break**
Poster Session 2: Defects and Metrology, New Materials, Slurry, Pad Conditioning
(all Posters in Poster Session 2 are listed on page 18)

Session 6: Metal CMP 2

Session Chairs:
Halbert Tam, JSR Micro;
Uwe Stöckgen, AMD

11:25 **Copper Oxidization Formation Analysis for Improving TDDB Reliability (Invited)**
Y. Yamada[1], Y. Yagi[2], N. Konishi[1], N. Ogiso[2], K. Katsuyama[1], S. Asaka[1], J. Noguchi[1], T. Miyazaki[2];
[1]Hitachi Ltd., Tokyo, Japan;
[2]Sanyo Chemical Industries Ltd., Kyoto, Japan

11:50 **Influence of Low-k Films on Barrier Removal Rate Variation Between Blanket and Patterned Wafers**
Y. Li[1], C. Burkhard[1], C. Wang[1], R. Wen[2], D. Mahulikaar[2];
[1]Clarkson University, Potsdam, NY, USA;
[2]Planar Solutions, Mesa, AZ, USA

12:10 **Evaluation of Cu CMP Barrier Slurries for Ultra Low-k Dielectric Film (k~2.4) for 45nm Technology**
F. Zhao[1], L. Economicos[3], W.-T. Tseng[2], H.-K- Kim[3], Edward Engbrecht[2], Jing Hui Li[1], Wu Ping Liu[1], M. Chae[4], L. M. Nicholson[4];
[1]Chartered Semiconductor Manufacturing Ltd.;
[2]IBM Systems and Technology Group;
[3]Samsung Electronics Co., Ltd.;
[4]Infineon Technologies AG

12:30 **Evaluation and De-coupling of Electrochemical and Mechanical Effects of Diluted WCMP Commercial Slurry on Tungsten Removal Rate**
D. M. Gianni[1,2], A. Mazzarolo[3], N. Masciocchi[2], A. Maspero[2], G. Spinolo[1], A. Vicenzo[3];
[1]STMicroelectronics, Agrate Brianza, Italy;
[2]Universita dell' Insubria, Como, Italy;
[3]Polytecnico di Milano, Milan, Italy

12:50 **Lunch / Coffee**
Poster Session 2: Defects and Metrology, New Materials, Slurry, Pad Conditioning
(all Posters in Poster Session 2 are listed on page 18)

Session 7: Defects and Metrology

Session Chairs:
Keiichi Kimura, Kyushu Institute of Technology;
Johann Wolfgang Bartha, Dresden Technical University

14:20 **Post-CMP Cleaning: Interaction between Particles and Surfaces (Invited)**
J.-G. Park; Hanyang University, Ansan, Korea

14:45 **Wafer Edge / Bevel Treatment of Device Wafers by Means of CMP**
A. Wieters, P. Thieme; Qimonda, Dresden, Germany

15:05 **Impacts on Microscratching in CMP Processes in High Volume Production**
G. Marxsen, S. Lingel, J. Schlott, A. Hoefgen; AMD, Dresden, Germany

15:25 **Oxide Thickness Profile Measurement by Dispersive White-Light Interferometry (Invited)**
H. Jeong[1], B. Park[1], Y. Kim[1], H. Kim[2], Y. Ghim[3], J. You[3], S. Kim[3];
[1]Pusan National University, Busan, Korea;
[2]Korea Institute of Industrial Technology, Busan, Korea;
[3]Korea Advanced Institute of Science and Technology, Daejon, Korea

15:50 **Coffee Break**
Poster Session 2: Defects and Metrology, New Materials, Slurry, Pad Conditioning
(all Posters in Poster Session 2 are listed on page 18)

Session 8: CMP Fundamentals 2

Session Chairs:
Ara Philipossian, University of Arizona;
Katrin Blum, IHP Frankfurt/Oder

16:45 **Full-Chip CMP Simulation System (Invited)**
D. Fukuda[1], T. Shibuya[1], N. Idani[2], T. Karasawa[2];
[1]Fujitsu Laboratoratories Ltd., Kawasaki, Japan;
[2]Fujitsu Ltd, Kawasaki, Japan

17:10 **Greenwood-Williamsson Model for Pattern-Dependent Planarization**
R. Rzehak, B. Vasilev; Qimonda, Dresden, Germany

17:30 **Study on Material Removal Phenomena in CMP Process**
K. Kimura[1], Y. Hashiyama[1], P. Khajornrungruang[1], H. Hiyama[2], Y. Mochizuki[2];
[1]Kyushu Institute of Technology, Fukuoka, Japan;
[2]Ebara Research, Kanagawa, Japan

17:50 **Modeling and Optimal Control of Chemical Mechanical Planarization**
S. Dürigen[1, 2], P. Benner[1], U. Stöckgen[2], J. Heinrich[2];
[1]Technical University Chemnitz, Germany;
[2]AMD Fab36, Dresden, Germany

18:10 **End of Sessions (Day 2)**

Friday, October 26, 2007
Poster Session 2
Defects and Metrology, New Materials, Slurry, Pad Conditioning

Development of Planarity Improved Abrasive-Free Copper CMP Slurry and Practical Non-Selective Barrier CMP Slurry Based on Electrochemical Study
J. Amanokura[1], K. Mabuchi[2], T. Sakurada[1], Y. Nomura[1], M. Habiro[1], H. Akahoshi[2];
[1]Hitachi Chemical Co., Ltd., Hitachi, Japan;
[2]Hitachi Ltd., Hitachi, Japan

The Organic Diamond Disk (ODD) for Dressing Polishing Pads of Chemical Mechanical Planarization
J. C. Sung[1], C.-S. Chou1, M. Sung[2] ;
[1]KINIK Company, Taipei, Taiwan;
[2]Advanced Diamond Solutions, San Francisco, CA, USA

Modeling for Pad Wear Control During Conditioning in CMP
T. Kasai, S. Anjur, H. Siriwardane; Cabot Microelectronics Corp., Aurora, IL, USA

The Fabrication of Ideal Diamond Disk (IDD) by Casting Diamond Film on Silicon wafer
J. C. Sung[1], Y.-T. Chen[2], M.-C. Kan[1], H.-K. Chang[1], M. Sung[3];
[1]KINIK Company, Taipei, Taiwan;
[2]National Defense University, Taoyuan, Taiwan;
[3]Advanced Diamond Solutions Inc., San Francisco, CA, USA

Three-Dimensional Metrology for CMP Process Evaluation with In-line Wide-Area Atomic Force Microscope
K. Murayama, T. Morimoro, Y. Kunitomo, M. Edamura, S. Sekino, T. Kurenuma; Hitachi-kenki Fine Tech Co., Ltd., Ibaraki, Japan

Pad Surface Microstructure and Optimization of the Conditioning Sweep
L. Borucki[1], X. Wei[2], Y. Zhuang[1,2], A. Philipossian[1,2], D. Slutz[3];
[1]Araca Inc., Tuscon, AZ, USA;
[2]University of Arizona, Tucson, AZ, USA;
[3]Morgan Advanced Ceramics, Allentown, PA, USA

Improvements of Electrical and Optical Property of Organic Light Emitting Diode Using Chemical Mechanical Polishing Process
G.-W. Choi[1], W.-S. Lee[1], Y.-J. Seo[2];
[1]Chosun University, South Korea;
[2]Daebul University, South Korea

Development of AE Monitoring System for CMP Process
S. Park[1], S. Joo[1], Y. Kim[1], H. Jeong[1], H. Kim[2];
[1]Pusan National University, Busan, Korea;
[2]Korea Institute of Industrial Technology, Busan, Korea

Reduction of Dishing in Polysilicon CMP for MEMS Application by Using Protective Layer and High Selectivity
W. Shin[1], S. Park[2], H. Kim[3], K. Park[1], H. Cho[1], S. Joo[1], H. Jeong[1];
[1]Pusan National University, Busan, Korea;
[2]University of California, Berkeley, CA, USA;
[3]Korea Institute of Industrial Technology, Busan, Korea

Experimental Analysis on CMP Mechanism of Single Crystal SiC
H. Lee[1], S. Jeong[1], H. Seo[1], B. Park[1], J. Oh[1], H. Jeong[1], H. Kim[2];
[1]Pusan National University, Busan, Korea;
[2]Korea Institute of Industrial Technology, Busan, Korea

Optimized and Customized CMP Conditioner Design for Next Generation Oxide/Metal CMP
T. Hwang, R. Vedantham, T. Puthanangady; Saint-Gobain High Performance Materials, Northboro, MA, USA

Impact in the Conditioning and Cleaning of Unwoven Fabric Polyester Pads with a High Pressure Micro Jet (HPMJ) on Silicon Polishing
K. Miyachi[1], Y. Seike[1], S. Haba[2], S. Kurokawa[3], T. K. Doi[3];
[1]Asahi Sunac Corp., Aichi, Japan;
[2]Nitta Haas Inc., Tokyo, Japan;
[3]Kyushu University, Fukuoka, Japan

Large Particle Counting for Quality Control of CMP Slurries
A. Nogowski[1], M. Stintz[1], H. Barthel[2];
[1]Technical University Dresden, Germany;
[2]Wacker-Chemie AG, Burghausen, Germany

Prime Wafer Geometry Improvement During Haze-free Polishing with Peter Wolters Polishing Head "M-Carrier"
J. Kanzow, M. Langenkamp, G. Mörsch; Peter Wolters AG, Rendsburg, Germany

Damascene Metal Gate Technology: A Front-end CMP Based Universal Platform for High-k Evaluation at the Device Level
R. Endres, U. Schwalke; Technical University Darmstadt, Germany

Defectivity Reduction in a Poly-Si CMP for SAFG Definition (in NOR Application)
L. Canevari, C. Romanelli, G. Spinolo, V. Bontempo; ST Microelectronics, Agrate Brianza, Italy

Development of Copper Post-CMP Cleaning Chemistries Compatible with Advanced Barrier Materials
D. Tamboli, M. Rao, G. Banerjee; Air Products and Chemicals, Allentown, PA, USA

Post-CMP Clean PVA Brush Design Advancements and Characterization in Cu/Low-k Applications
R. K. Singh, C. R. Wargo, D. W. Stockbower; Entegris Inc., Billerica, MA, USA

Laser Scattering Technique for Characterizing Defects and Surface Morphology in the Fixed Abrasive CMP Process
J. Gagliardi[1], E. Olson[1], U. Mahajan[2,] H. Zhang[2,], C. Douglas[2,];
[1]3M Corporation, St. Paul, MN, USA;
[2]KLA-Tencor Corporation, Milpitas, CA, USA

Enhanced Control and Manufacturing for CMP Processing with Advanced Blending and Delivery of Slurries
G. Liu, R. Moulton, L. Han, G. Flores; ChemFlow Systems Inc., San Jose, CA, USA

Conditioning of CMP Pad to Reinstate Pad Surface Function
K. Kadomura[1], T. Fukunishi[2,], Y. Umezaki[3], S. Kurokawa[3], T. Doi[3];
[1]A.L.M.T. Diamaond Corp.; Hyogo, Japan;
[2]A.L.M.T. Corp., Hyogo, Japan;
[3]Kyushu University, Fukuoka, Japan

Effect of Diamonds on Pad Recovery in Oxide and Metal Pad Conditioning Process
B.-K. Kang[1], Y.-J. Kang[1], K.C. Kim[1], J.-G. Park[1] J.-H. Lee[2,], J.-S. Ahn[2,];
[1]Hanyang University, Ansan, Korea;
[2]Ehwa Diamond Ind. Co., Ltd., Osan, Korea

Accelerating Development Timeframes Through Effective Use of CMP Outsourcing
R. Carroll[1], L. Rhoades[2,];
[1]Polar Semiconductor Inc., USA;
[2]Entrepix Inc., Tempe, AZ, USA

Point of Use Quality Control of CMP Slurries
F. Hinze, J. Altmann; Aello, Dresden, Germany

Optimizations of Post Polish Procedure for Defect Density Reduction
H. Lauber, S. Muenzberger; Infineon Technologies, Dresden, Germany

Fabrication of Surface Acoustic Wave Structures with buried Copper IDTs using the Copper Damascene Process
S. Menzel[1], D. Reitz[1], U. Künzelmann[2], M. Albert[2], J.-W. Bartha[2];
[1]Leibniz-Institute for Solid State and Materials Research (IFW), Dresden;
[2]Dresden University of Technology, Dresden, Germany

Material & Design Considerations for Zero Defect CMP Pads
R. Carpio[1], F. Tolic[1], S. Hymes[2], R. Bajaj[2];
[1]ATDF, Austin, TX, USA;
[2]SemiQuest Inc., San Jose, CA, USA

Saturday, October 27, 2007

Social Day
"World Heritage Discovery Tour"

Experience the Dresden Elbe valley from the land, from the air and from the water. During a combined walking and coach tour, we would like to introduce a cultural landscape which has evolved over the course of 800 years. Learn more about the famous sights of the city, such as the Zwinger, Semper Opera House and Frauenkirche. The journey continues past broad green meadows and below the so-called Elbe palaces to the oldest suspension railway in the world.

From the Loschwitz Heights, you can enjoy a magnificent view over the whole Elbe valley. The next stopping point is no less fascinating: Pillnitz Palace and Park. During a tour of the complex, you will become acquainted with the history, architecture and landscape gardening of this unique integral work of art. Alongside the dendrological treasures of the park, we will also show you around one of its pavilions, the Catholic palace chapel and the historical palace kitchens. During the return journey to Dresden aboard a paddle-steamer, you can relax and absorb once more the harmony of urban and natural landscapes.

09:00 h	Tourist Guide starts the walking tour at the Theaterplatz/Reiterdenkmal near the Semper Opera House
16:45 h	End of tour at the Elbeterassen

Please make your registration in good time. Bookings for excursions will be made on a "first come - first served" basis upon receipt of registration and payment.

The total amount shall be paid in advance or at the registration desk and has to be made in EUR.

CONFERENCE INFORMATION

CONFERENCE HOURS

Thursday, October 25, 2007	09:00 h to 18:40 h
Friday, October 26, 2007	08:30 h to 18:10 h

REGISTRATION HOURS

Wednesday, October 24, 2007	17:00 h to 19:00 h
Thursday, October 25, 2007	07.30 h to 09:30 h

EXHIBITION

The two-day tabletop exhibition is an integral part of the ICPT 2007 conference and takes place at an exhibition area close to the conference lecture room which can be visited during all coffee and lunch breaks.

Exhibition space of 4 m^2 or 6 m^2 (40 sqft or 60 sqft) with table, two chairs and poster board are available. Registration for the exhibition includes two full access badges, two copies of the proceedings and a company name listing in all promotional materials.

For further information on the exhibition please contact
Dr. Ronald Schnabel
Stresemannallee 15
D-60596 Frankfurt am Main, Germany
Phone: ++49-69-6308-330, Fax:++49-69-6308-9828
E-Mail: gmm@vde.com

INFORMATION FOR AUTHORS

MANUSCRIPTS AND PROCEEDINGS

Manuscripts should be send to conference-papers@vde.com by **August 24, 2007**. Since the manuscripts will be directly reproduced in the proceedings please send a pdf-file by e-mail. The manuscripts are limited to 6 pages (figures included). When writing respectively shaping your manuscript, please observe the "Instructions for paper preparation", which you will find at http://www.ICPT2007.com

The conference proceedings and CD-ROM will be published by the VDE/VDI Society Microelectronics, Micro- and Precision Engineering and will be delivered to the conference participants at the registration desk.

Please note that late submissions may not be considered in the conference proceedings.

GENERAL INFORMATION

ICPT 2007 SECRETARIAT

For detailed Information please contact:

VDE/VDI-Society Microelectronics, Micro- and Precision Engineering (GMM)
Dr. Ronald Schnabel
Stresemannallee 15
D-60596 Frankfurt am Main, Germany
Phone: ++49 69 / 6308-330
Fax: ++49 69 / 6308-9828
E-Mail: gmm@vde.com
During the conference:
Phone: ++49 171 4695 118

CONFERENCE FEES

	until **Sept. 25,2007**	after **Sept. 25,2007**
Non-Members	€ 390,00	€ 440,00
VDE, VDI-Members*	€ 350,00	€ 400,00
Lecturer	€ 350,00	€ 400,00
Exhibitor (max. 2 people)	€ 0,00	€ 0,00
Non-Member-Students**	€ 40,00	€ 70,00
Student Members**	€ 20,00	€ 50,00
Extra proceedings	€ 60,00	€ 60,00
Discovery tour 27.10.2007	€ 70,00	€ 70,00

* Participants applying for the membership fee must include a copy of their membership card to the registration form.
** A photocopy of the student card must be included.

The conference fee includes admission to all sessions as well as to the daily coffee-breaks and lunches, one copy of the proceedings including a CD-ROM, conference dinner on Thursday.

CONFERENCE REGISTRATION

To register for ICPT 2007 please fill in the registration form attached to this program and return to VDE Conference Services, Stresemannallee 15, 60596 Frankfurt, Gemany. To enjoy the “early-bird-discount”, VDE Conference Services must receive the form before September 25th, 2007. Full payment or credit card information must accompany all registrations in order to be accepted. Completed forms may be sent by fax (+49 69 96 31 5213) surface mail or e-mail (vde-conferences@vde.com). A confirmation of the registration will be sent upon receipt of full payment.

ONLINE REGISTRATION

Registrations for the conference may be done online on the conference homepage www.icpt2007.com

PAYMENT TO THE VDE/VDI SOCIETY

Payment for registration, including bank charges and processing fees, must be made in Euro.

The conference fee has to be fully paid in advance. Confirmation of registration will be sent after full payment has been received at the VDE-Conference Services.

The following methods of payment are accepted:

- Cheque in EURO (€) payable to VDE and sent together with the registration form by mail.
- By credit card authorisation as per registration form. The 16 digit card number, expiry date, security No. (last 3 digits on rear side of credit card) and holder's name must be indicated on the registration form. Signature of the card holder is mandatory.
- Cash payment on-site in EURO (€)

CANCELLATION

In case of cancellation, provided that written notice is received at the VDE-Conference Services before Sept. 25, 2007, the registration fee will be fully refunded less a handling fee of EURO 60,00. After Sept. 25, 2007 no refund will be made. Proceedings and CD-ROM will then be sent to the registrant after the conference.

PROCEEDINGS

All papers accepted for presentation at the conference will be published with the proceedings and a CD-ROM. The proceedings will be handed on-site to all delegates attending the event.

Additional proceedings and CD-ROM are on sale during the conference (upon availability) at EURO 60,00

CONFERENCE VENUE

Hilton Dresden
An der Frauenkirche 5
D-01069 Dresden, Germany
Phone: +49 351/86420
Fax: +49 351/8642-725

Hilton Dresden, located in the heart of the old town, next to the Frauenkirche, is situated on Bruehl's Terrace. The Semper Opera House and the world-renowned "Zwinger" are within walking distance. The piers of the world's largest and oldest paddle steamer fleet are next to the hotel.

HOTEL RESERVATION

A block of rooms has been reserved for ICPT 2007 participants

Hilton Hotel Dresden

The hotel room rate (special rate, including breakfast) is

165,00 EURO (single room classic),
190,00 EURO (double room classic)

190,00 EURO (single room deluxe),
215,00 EURO (double room deluxe)

220,00 EURO (single room executive),
245,00 EURO (double room executive)

per night. Accomodation is not included in the conference fee. Please contact the Hilton Hotel, for reservation.

Hilton Dresden
An der Frauenkirche 5
D-01069 Dresden, Germany
Phone: +49 351 / 8642-0
Fax: +49 351 / 8642-725
E-Mail: info.dresden@hilton.com
http://www.hilton.com/

You should reserve your room by September 12th, 2007 or our block of rooms at the Hilton Hotel may be released by the hotel for general sale. Please use the following code for booking: “ICPT 2007”

Ramada Hotel Dresden

The hotel room rate (special rate, including breakfast) is

93,00 EURO (single room comfort),
107,00 EURO (double room comfort)

per night. Accomodation is not included in the conference fee. Please contact the Ramada Hotel for reservation.

Ramada Hotel Dresden
Wilhelm-Franke-Straße 90
D-01219 Dresden, Germany
Phone: +49 351 / 4782-0
Fax: +49 351 / 4782-550
http.// www.ramada-dresden.de

You should reserve your room by August 24th, 2007 or our block of rooms at the Ramada Hotel may be released by the hotel for general sale. Please use the following code for booking: “ICPT 2007”

All payments related to accommodation have to be made directly on departure in the hotel.

BUSSHUTTLE

There will be a busshuttle from the Ramada Hotel to the Hilton Hotel on both conference days. The bus will depart half an hour before the beginning of the conference on Oktober 25 and 26, 2007.

INSURANCE

The organisers may not be held responsible for any injury to participants or damage, theft and loss of personal belongings.

PASSPORT AND VISA REQUIREMENTS

Foreign visitors entering Germany have to present a valid Identity Card or Passport. Delegates who need a visa should contact the German consular offices or embassies in their home countries. Please note that neither the VDE-Conference Services nor the VDE/VDI-Society Microelectronics, Micro- and Precision Engineering (GMM) or the supporting bodies are able to extend any "Invitation" for application of visa.

TRANSPORT

By Air

Dresden Airport
Distance from hotel: 10 km, Drive time: 20 min.
Directions: Follow signs to city centre. After passing the Elbe Bridge, turn right onto Terrassenufer. Follow Hilton signs.

Getting to and from the airport

Bus Service, typical minimum charge is EURO 8,00
Limousine, typical minimum charge is EURO 70,00
Taxi, typical minimum is EURO 25,00

By train

from Frankfurt in 5 hours
from Berlin in 3 hours

LIST OF EXHIBITORS

3M Company, St. Paul, USA
Abrasive Technology, Ohio, USA
AGC Electronic Materials, Hillsboro, USA
Araca, Inc., Tucson, US
ATDF, Inc., Austin, USA
Cabot Microelectronics, Aurora, USA
ECO Physics AG, Dürnten, Suisse
Ehwa Diamond Ind. Co. Ltd., Osan, Korea
Entegris GmbH, Dresden, Germany
Euris GmbH, Tübingen, Germany
G&P Technology, Inc., Busan, Korea
JSR Micro N.V., Leuven, Belgium
Kemesys,Peynier, France
Mitsubishi Materials Corp., Tokyo, Japan
Morgan Advanced Ceramics, San Jose,USA
Pall GmbH, Bad Kreuznach, Germany
Qimonda AG, Dresden, Germany
Rohm und Haas Electronic Materials, Dresden, Germany
Samsung Cheil Industries Inc.,Uiwang-Si,Geyoinggi-Do, Korea
Shinan Diamond Industrial Co., Ltd., Incheon, Korea
SPS-Europe B.V., Putten, The Netherlands
Struers GmbH/Logitech Ltd, Willich, Germany
Umicore, Olen, Belgium

Notes

Notes

The IPCT 2007 Organizing Committee would like to express its sincere appreciation to the following companies for their support: