Integration Issues and Challenges for Copper Low K Processes

Ajoy Zutshi
Applied Materials

The use of Copper in logic applications has been successfully been implemented for 130 nm geometries. However, the integration of Copper into the flow has been a challenging and troublesome issue. The use of Copper also requires damascene processing, which adds additional complexity in etch and CMP processes. In addition to this, the technology leaders are trying to introduce dielectric films with low dielectric constants. Typically, low K materials have much lower mechanical properties, and this poses new challenges in developing appropriate integration schemes.

Several aspects of Copper Low K integration can be discussed, starting from deposition of low k films to the polishing of the copper-low k wafers to produce the desired output.

Deposition requires precise control of the CVD process (or spin on process) to provide the film with optimal mechanical and dielectric properties so that a) the film can withstand the level of shear and normal stresses during the CMP process, b) the dielectric constant of the material is as desired and c) the film surface can be adequately cleaned to provide a defect free surface.

Etch processes require control of the critical dimension (CD) of the smallest geometries as well as the depth of the vias and trenches with the appropriate aspect ratios. The CD and trench depth, i.e. cross sectional area determine the metal line resistance and current carrying capability of the particular line.

The metallization processes of barrier and electroplating have significant challenges in terms of filling the vias and trenches, void free and with appropriate uniformity

As is well understood, CMP is a combination of mechanical and chemical forces to remove material layer. Copper and Copper oxide as a polishing material is significantly softer than Tungsten or SiO_2 films, hence typically copper CMP processes are centered at about 3-5 Psi vs 5-8 Psi for SiO_2 CMP processes used before. With the introduction of low k materials, which are typically 60-70% softer than SiO_2 films, the polishing process needs to be significantly modified to accommodate these materials. One way of doing this is to reduce the mechanical aspect of polishing and decrease the chemical component of polishing, without compromising the planarization efficiency of the polishing process.

This paper will discuss various aspects of process integration for Copper Low K materials. A discussion will be presented with challenges for process integration and some unique ways to resolve these challenges.