TCAD Modeling for Mechanical Stress Management in 3D IC Packages

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Outline

• Thermal Mismatch Stresses in 3D IC

• Modeling stress evolution with TCAD

• Analyzing stress effects on performance and reliability

• Stress management in 3D IC technology integration and design
Through Silicon Via Stress Effects

- **Reliability**
  - Pumping

- **Mobility change**
  - Radial tension
  - Circumferential compression

- Via material, process
- Silicon crystal orientation, P/N
- Barrier layer material
- Insulation liner material and thickness
- TSV pitch, diameter

Performance shifting due to TSV stress
- IMEC, VLSI 2010

TSV extrusion and de-lamination
- Tezzaron, RTI 2009

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Thermal Mismatch Stress near u-bump

Micro-bump Array

Deformed Micro-bump

Active region

\[ \alpha_{\text{under-fill}} > \alpha_{\text{bump}} \]

Thermal mismatch leads to die pull-down and bump push-up
Micro-bump Stress Effects

• Micro-bumps introduce stresses that depend on
  ▪ Micro-bump and under-fill material properties
  ▪ Micro-bump geometry and layout parameters

• Micro-bump stress effects
  ▪ Current shift in devices above micro bumps
  ▪ Interface delamination and cracking

Interface cracking near micro-bump

Device On current shift above micro-bump
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TCAD 3D IC Simulation Flow

Process Info

Deposit  material=Oxide thickness=0.3 type=isotropic
Etch  mask=metal_2 material=Oxide thickness=0.3

Layout Info

Process Simulation
Finite Element Analysis

Model Selection

Material Property

3D Structures
Solution Fields
Mobility Variations
Reliability Analyses

Effective Stress
Reliability
Mobility Variation

**TSV and μ-bump Stress Simulation**

**Via-middle process:**

1. FEOL → TSV → BEOL → Thinning → Backside → μ-Bump → Stacking

**Layout**

After TSV step

After stacking step

**After bump step**

Bottom die (Die 1)

Top die (Die 2)

Bottom die (Die 1)

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Stress Evolution with Process Steps

After TSV step

After micro-bump step

Die 1

100 MPa

5.4 um

TSV

Die 1

100 MPa

3.3 um

Sxx (Pa)

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Synopsys, 12th Int. Workshop on Stress in Microelectronics, 2012
Material Behaviors in TSV Stack

- Top die (Die 2)
- Bottom die (Die 1)
- BEOL
- RDL Oxide
- TSV
- Micro-bump
- Under-fill

**Material Behavior Details**

- **Anisotropic elastic**
  - Silicon

- **Visco-elastic**
  - Under-fill

- **Cohesive Interface**
  - Material strength vs. De-bonding energy

- **Visco-plastic**
  - Solder

- **Orthotropic elastic**
  - BEOL

- **Elastic-plastic**
  - Copper

Synopsys, 12th Int. Workshop on Stress in Microelectronics, 2012
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P-mobility Variation on Die-1 Surface

Stress around TSV
- Radial tension
- Circumferential compression

- Mobility variation localized around TSVs
- Keep-Out-Zone (KOZ) design rule and place & route methodology

Synopsys, 12th international workshop on stress-induced phenomena in microelectronics, 2012
TSV Diameter and Pitch Effects

TSV Diameter = 5 um

TSV Diameter = 10 um
~38% higher normal stress

Synopsys, 12th international workshop on stress-induced phenomena in microelectronics, 2012
N-mobility Variation on Die-2 Surface

- Mobility variation localized above u-bump
- KOZ design rule and place & route methodology

Synopsys, 12th international workshop on stress-induced phenomena in microelectronics, 2012
Under-fill CTE Impact

LCTE: 15.0, 30.0 and 45.0 ppm/°C

Larger under-fill CTE leads to greater mobility variation

Active region

Large under-fill CTE increases contraction and pulling down

Synopsys, MRS Proceedings, 2011
Copper Anisotropic Effect on Crack

- Crack driving force and mode mixity depends on copper anisotropy in different crystal orientation

<table>
<thead>
<tr>
<th>Anisotropic Copper</th>
<th>E1</th>
<th>E2</th>
<th>E3</th>
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<tr>
<td>Anisotropic 1</td>
<td>156 GPa</td>
<td>69 GPa</td>
<td>69 GPa</td>
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<tr>
<td>Anisotropic 3</td>
<td>69 GPa</td>
<td>69 GPa</td>
<td>156 GPa</td>
</tr>
</tbody>
</table>

Synopsys/Fraunhofer, IEEE TDMR, 2012
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Managing KOZ with TCAD Modeling

M. Rabie, et al, GLOBAL FOUNDRIES, IITC 2014

- Tensile stress due to TSV copper shrinkage is compensated by compressive stress due to CMP stop layer
- Experiments and TCAD simulations
Stress Management at Qualcomm

TSV Effect

μ-Bump Effect

Stacking Effect

Qualcomm, CICC 2010, ECTC 2014
Summary

• Mechanical stress in TSV stacks affects both performance and reliability

• TCAD modeling of stress evolution and stress effects provides valuable insights

• 3D IC design and technology configurations can be optimized with stress management