WaferMasters, Inc.

New Technology for Thermal Processing

By John Foggiato

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Outline

- Issues with RTP
- How WaferMasters Addressed the Issues
- Various Characterized Processes
- Future Directions

Dependence of Light Intensity on Temperature

Heat Source

Pyrometer

Temperature Readout

Wavelength

3.0μm

0.96μm

5.3μm

Intensity (Arb. Unit)

100
80
60
40
20
0

0 200 400 600 800 1000 1200 1400

Temperature (ºC)

Filtered IR Image

as is

(2000.0)
1490.0
M.Point
a:1099.7
(200.0)

Filter

Heat Source

Pyrometer 3~5.3μm

Si 0.7mm

(2000.0)
1490.0
M.Point
a: 648.0
(200.0)

Si 1.4mm

(2000.0)
1490.0
M.Point
a: 440.9
(200.0)

Si 2.1mm

(2000.0)
1490.0
M.Point
a: 322.9
(200.0)

Effect of Filters on Temperature Measurement

Measured Temperature (°C)

1200
1000
800
600
400
200
0

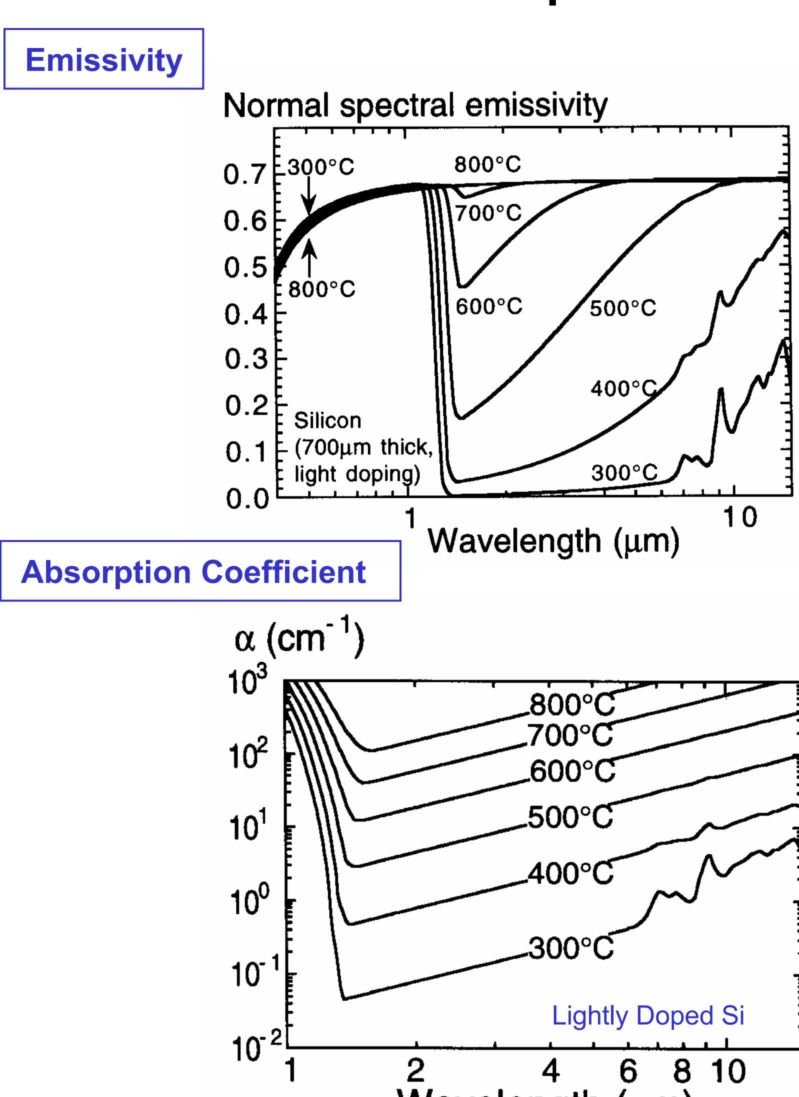
Detection Limit
for 0.96μm

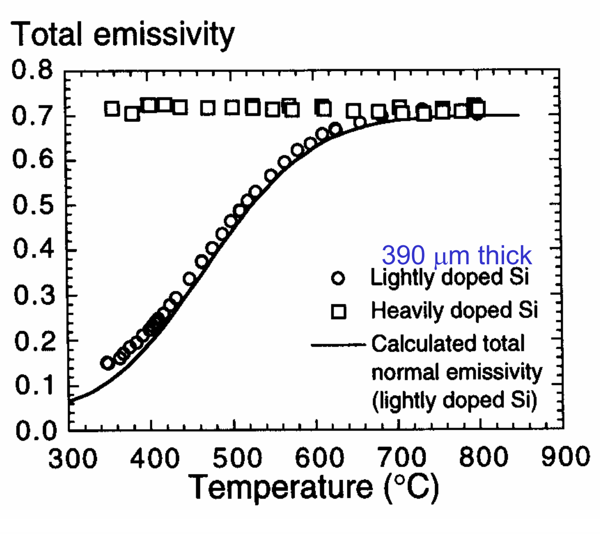
None
0.7mm Si
1.4mm Si
2.1mm Si
0.5mm Quartz
1.5mm Quartz
5.0mm Quartz
5.0mm Quartz (Blasted)

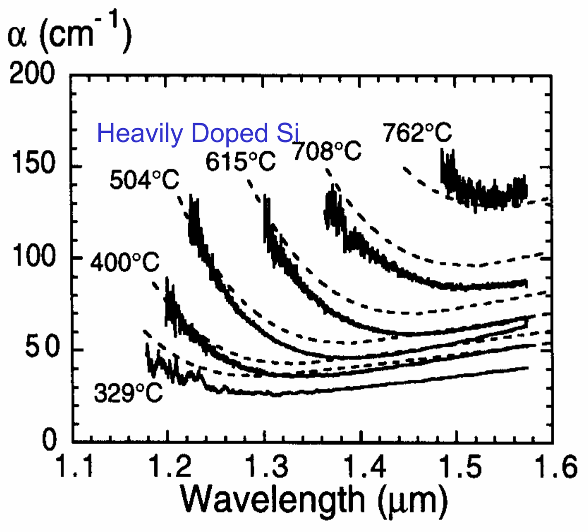
Filter Used

0.96μm
3.0~5.3μm

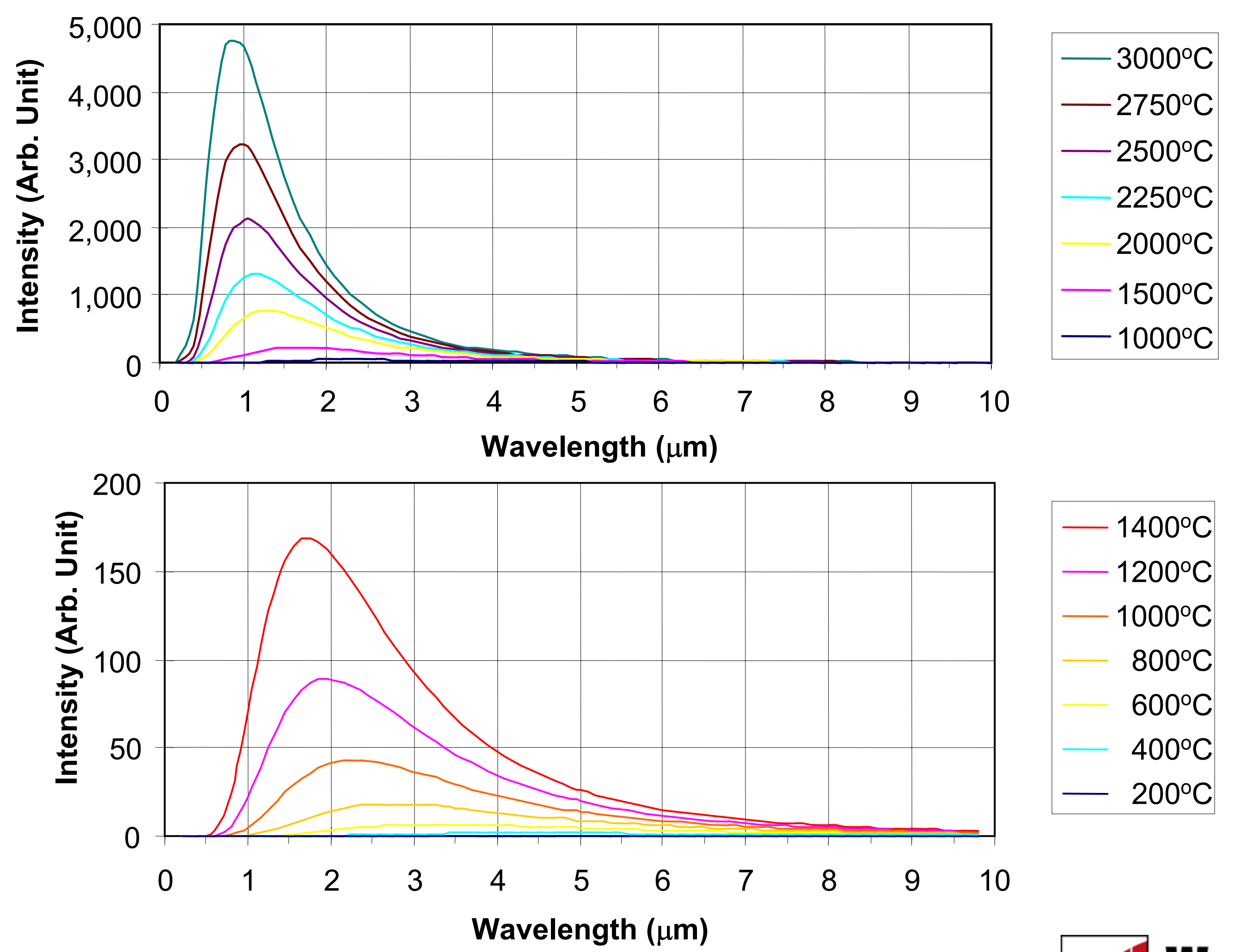
Optical Properties of Si







Radiation Spectra from Heated Blackbody



WaferMasters
Incorporated

Spectral Features in Thermal Processing

Blackbody Radiation

Intensity (Arb. Unit)

200
150
100
50
0

0 1 2 3 4 5 6 7 8 9 10

Wavelength (μm)

1400ºC
1200ºC
1000ºC
800ºC
600ºC
400ºC
200ºC

Quartz

Si

Transmittance (%)

100
80
60
40
20
0

Absorption Coefficient (cm^{-1})

50
40
30
20
10
0

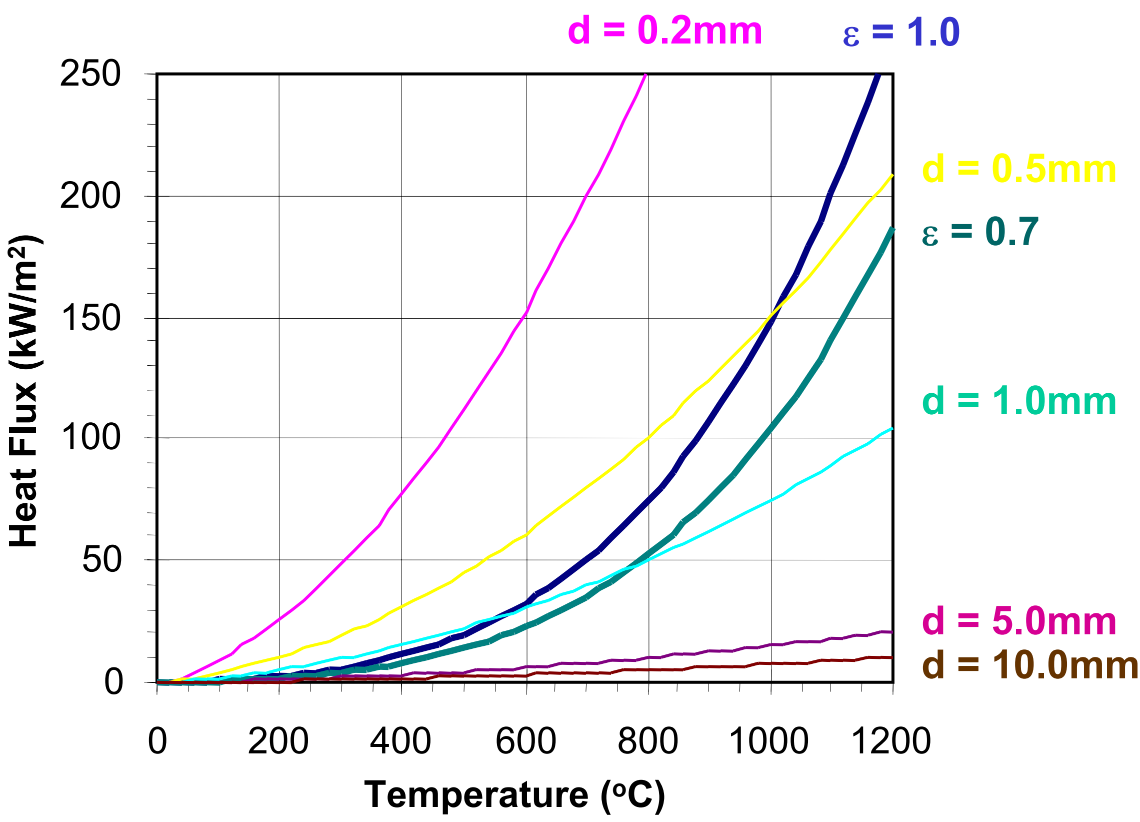
0 1 2 3 4 5 6 7 8 9 10

Wavelength (μm)

Wafer Heating Mechanism

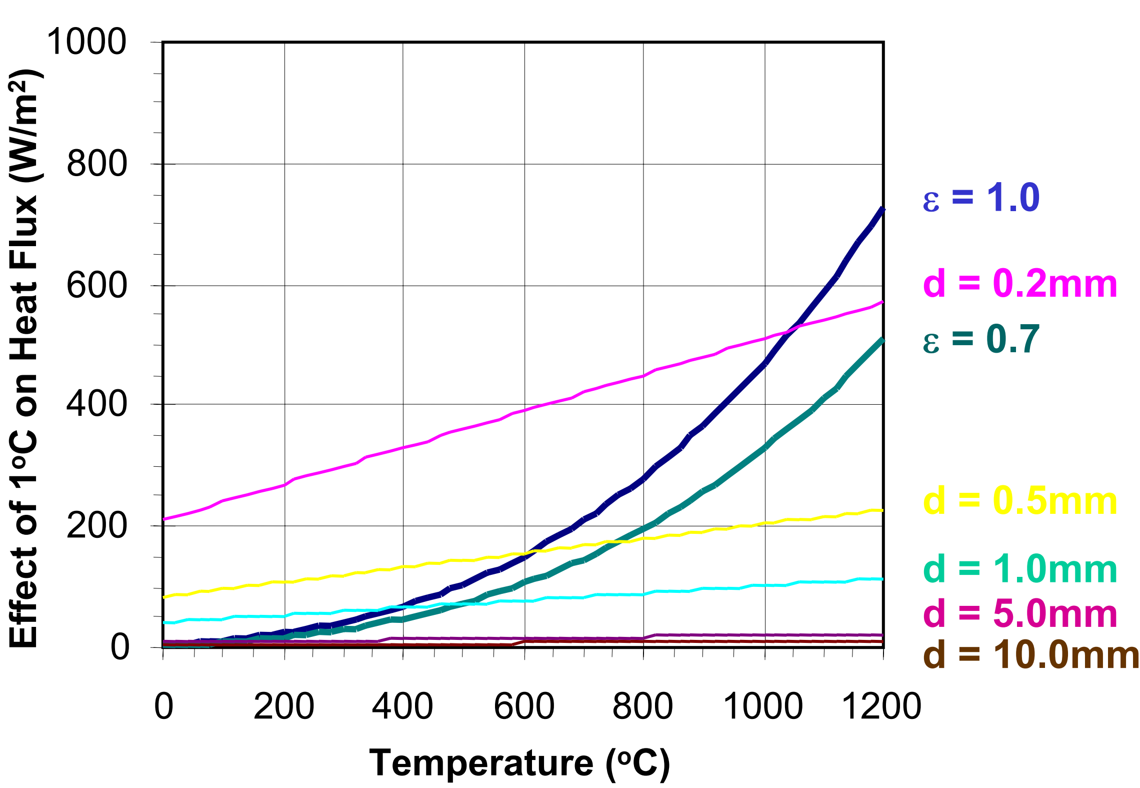
Radiation vs. Conduction

$W(T) = \varepsilon \sigma (T_a^4 - T_b^4)$ $W(T) = \lambda (T) (T_a - T_b)/d$



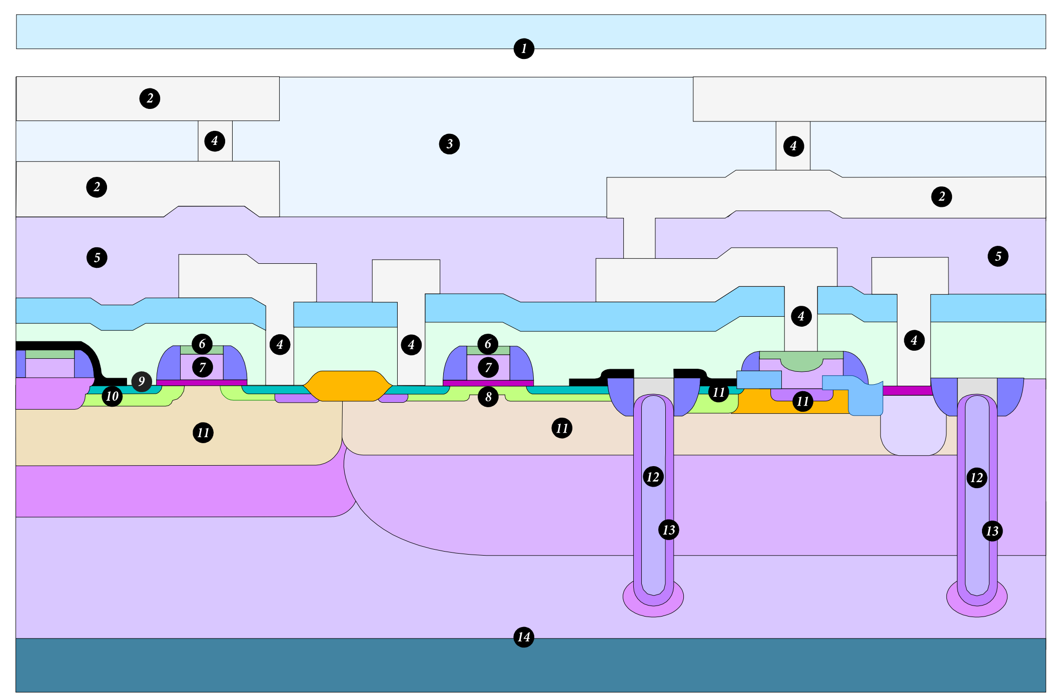
Impact of 1°C on Wafer Heating

Radiation vs. Conduction



Applications of RTP in Semiconductor Device Manufacturing

1. Polyimide Curing
2. Metal Anneal
3. Low-*k* Interlevel Dielectric
4. Curing of Photo Process Planarization Materials
5. Interlayer Dielectric Densification
6. Silicide Formation
7. Gate Electrode Anneal
8. High-*k* Dielectric Densification
9. Thin Oxide Growth
10. Ultra-Shallow Junction Activation and Anneal
11. Well Implant Anneal
12. Oxide Trench Fill Densification
13. Trench Oxidation and Corner Rounding
14. SOI Splitting



How WaferMasters, Inc. Addressed Issues

- Isothermal Chamber-No backside pattern effects
- Utilized Natural Characteristics of Wafers' Thermal Capacity
- Wafer Handling
- Wafer Temperature Control/Uniformity
- No Moving parts-Contamination Control
- Small Footprint and Low Power and Gas Consumption

“Single wafer Rapid Thermal Furnace”

SRTF

Process Module of High Temperature SRTF

Thermal Insulator 2
Thermal Insulator 1
Load lock
O_2 + N_2
Heat Diffuser
Heating Elements
Zone 1
Zone 2
Zone 3
Thermal Insulator
TC1
TC2
TC3
Exhaust
Temperature Controller
Zone 1 Power
Zone 2 Power
Zone 3 Power
Data
TC for Wafer Temp. Monitoring
Computer

- Resistive Heating
- Minimum Aperture (d << W, d << L)
- Nearly Isothermal Cavity
- No Moving Parts
- Zone Temp. Control
- Heat Diffuser
- Wafer Temp. Monitoring

Single Wafer Rapid Thermal Furnace Configuration

AGV Interface

Vacuum Loadlock

Process Chambers

Robot

Cooling Stations

Robot

Chamber 2

Chamber 1

New or Processed Cassettes

Vacuum Pump

Configuration of Lower Temperature Chambers

Process Module
- Stacked Hot Plates

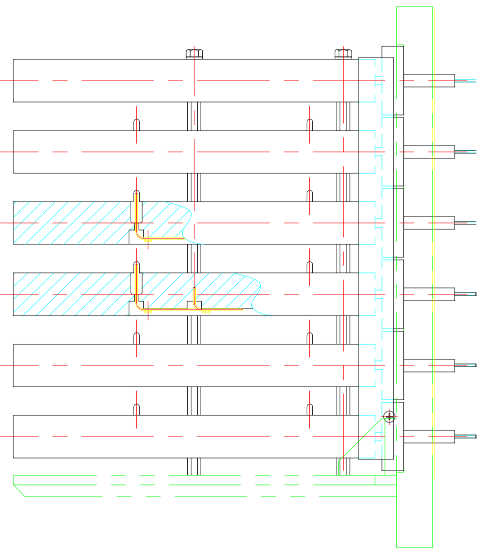
Load Port
- Triangular door

Optical Bench
- No adjustment

Vacuum Robot
- Extended z-axis travel

Cassette Stage
- Cooling stations

Vacuum Pump
- Integrated



X-ray Topography with Optimal End Effector

Wafer Processed 5 times at 1100°C, 60s under 1 atm air

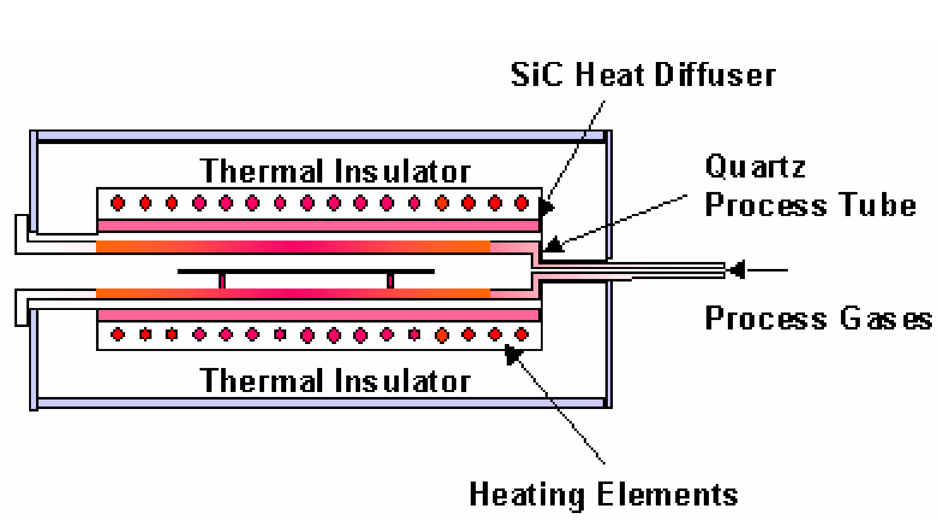
slip
standoff
end effector
standoff
a

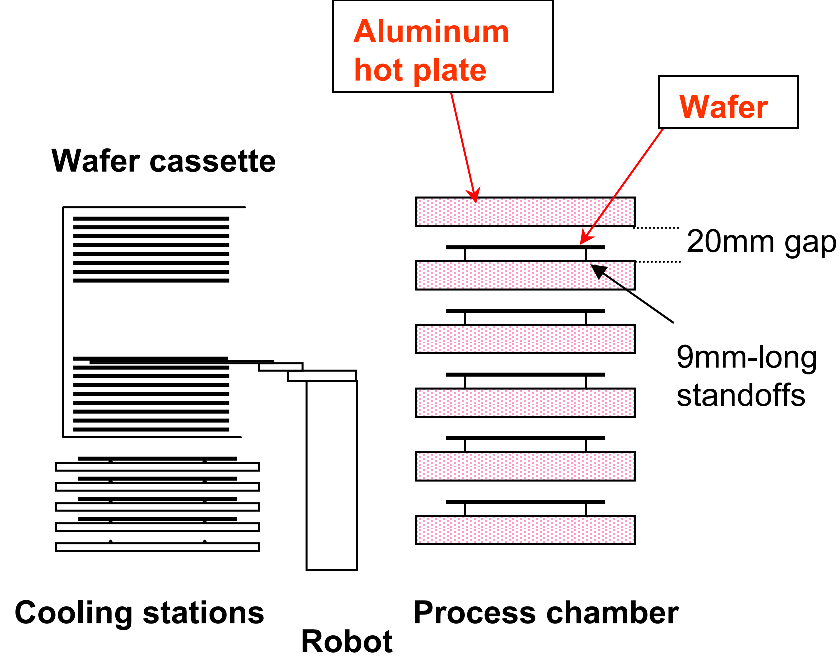
slip
b

c

d

System Configurations for Metal Silicide Formation

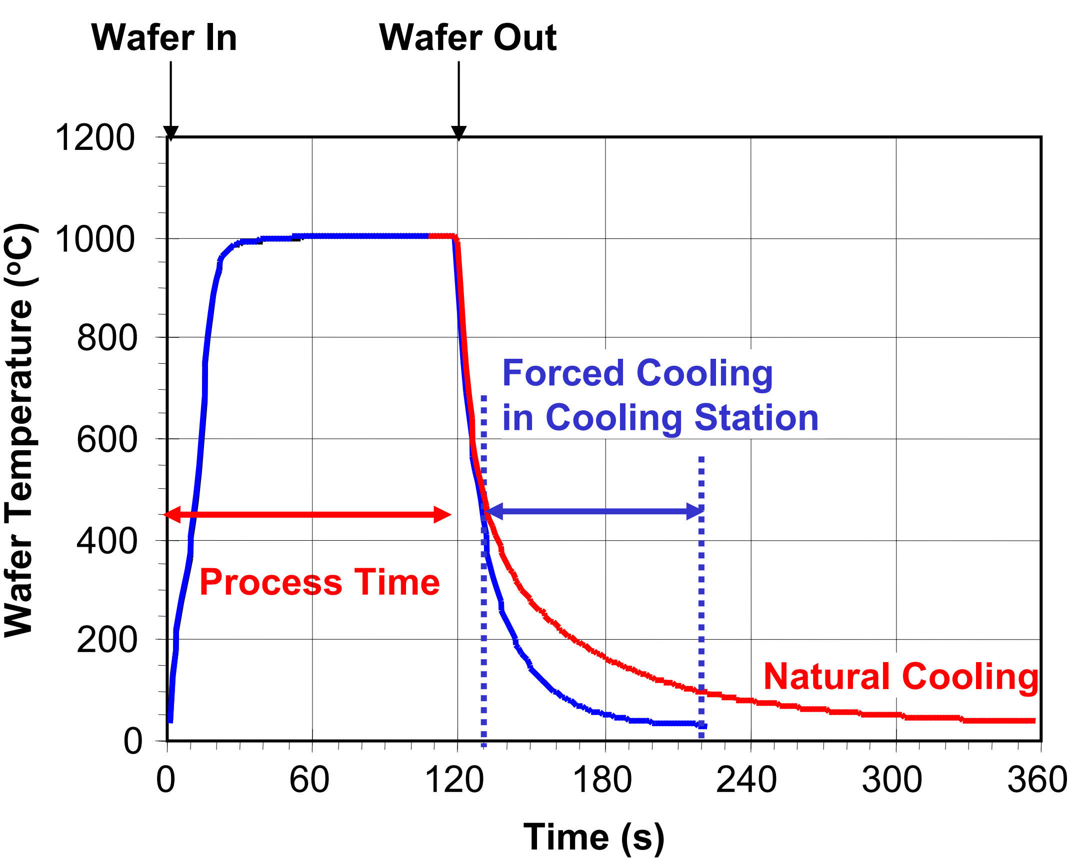




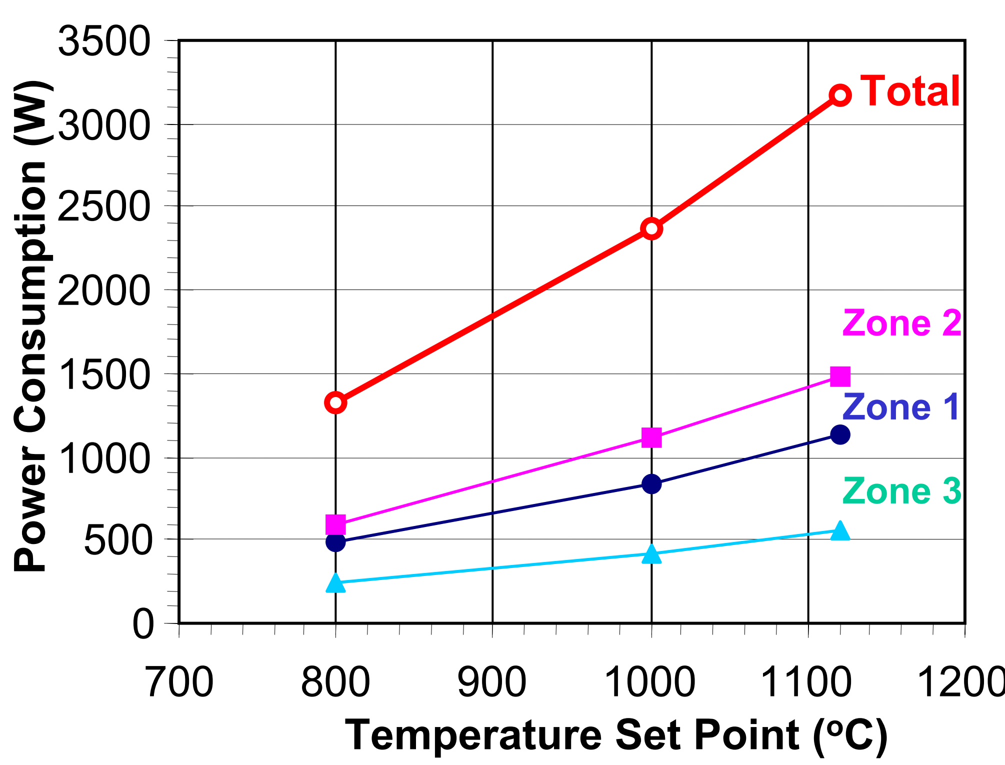
SRTF-200LP
- -No moving parts in process chamber
- -Temperature range : 200 – 1100°C

SAO-200LP
- -Individually controlled heater element
- -Temperature range : 100 – 550°C

Wafer Heating and Cooling Capability



Low Power Consumption



Thermal Product Road Map

150 to 300 mm wafers

Flash

SRTF

MBF

SAO

DCH

Temperature (°C): RT, 200, 400, 600, 800, 1000, 1200

Process Time: Momentary, 1 min, 5 min, 10 min, 20 min, 30 min

H_2 Anneal
Oxidation
Implant Anneal
USJ Anneal
Nitridation
Glass Reflow
Film Densification
Silicidation (2nd step)
Ta_2O_5 Recrystallization
Silicidation (1st step)

SOI Splitting
Al Sintering
Ta_2O_5 Deposition
Wafer Bumping
SOG/SOD Anneal
Cu Anneal
Photoresist Bake

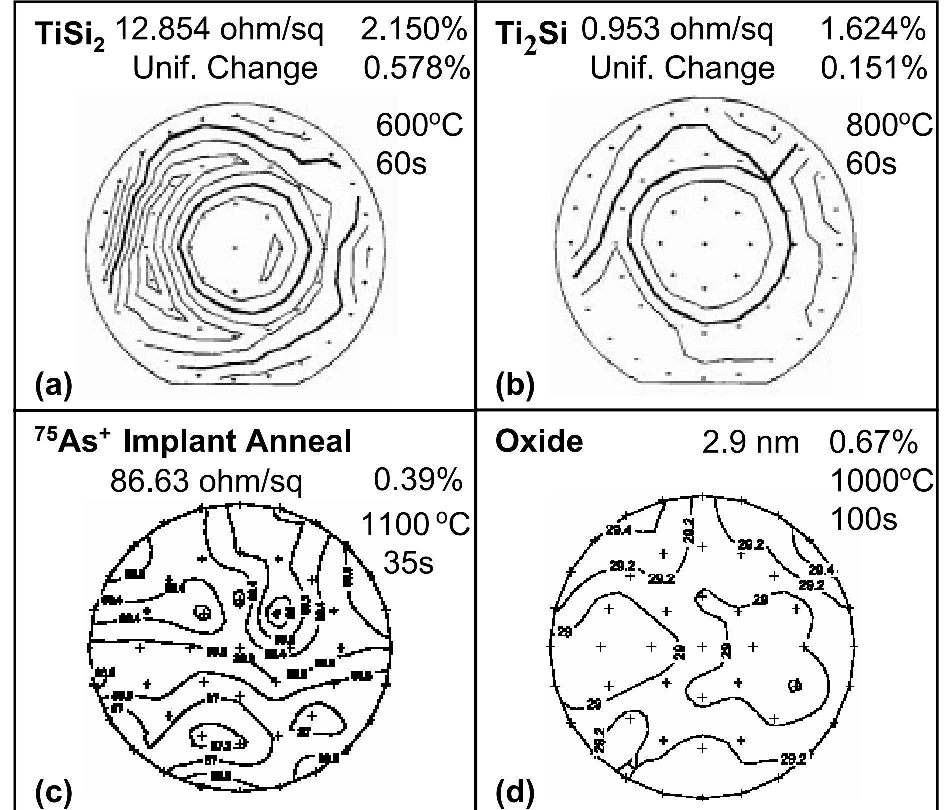
Flash: Flash Annealing System
SRTF: Single Wafer Rapid Thermal Furnace (Sold Through TEL)
DCH: Direct Contact Hot Plate System
SAO: Stacked Annealing Oven
MBF: Mini Batch Furnace

Typical Process Uniformity

$TiSi_2$ Formation

Implant Anneal

^{75}As 70keV 1E15



Ti_2Si Formation

Dry Oxidation

200mm Stacked Annealing Oven

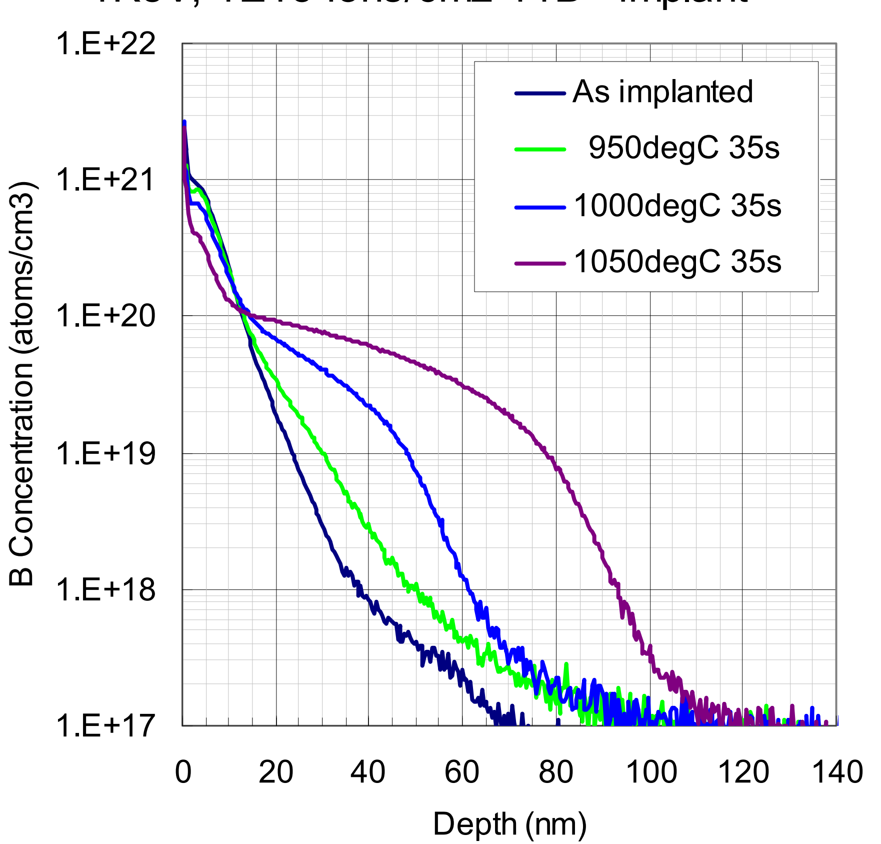
600mm (W) X 1200mm (D) X 1700mm (H) (2 ft X 5 ft X 6 ft)

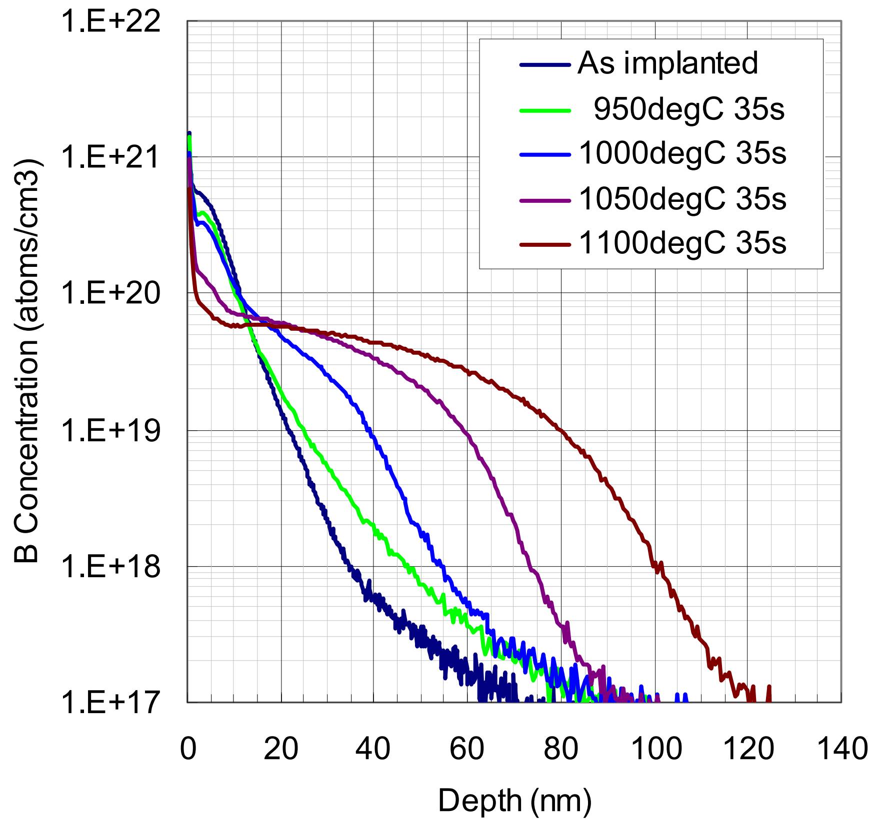
SRTF-300AP System

Various Characterized Processes

- Ion Implant
  - Boron, BF2 and with amorphization Species
  - Phosphorus and Arsenic
- BPSG Reflow
- Silicide Formation
  - TiSi, CoSi, NiSi
- Low Temperature Anneals
  - Copper
  - SOG
- Film Growth
  - Oxide, Nitride
- Defect Engineering

SIMS Profiles of 35sec Process Temperature dependence



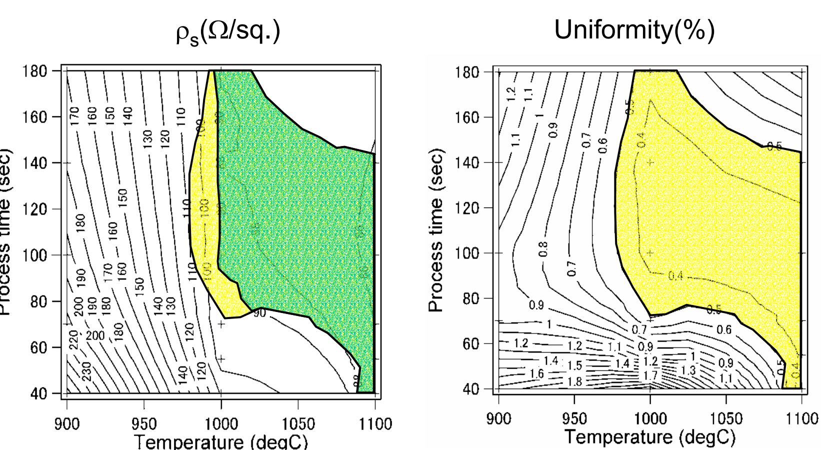


Ion Implant Anneal Process Window Comparison

Uniformity <0.5%(1σ)

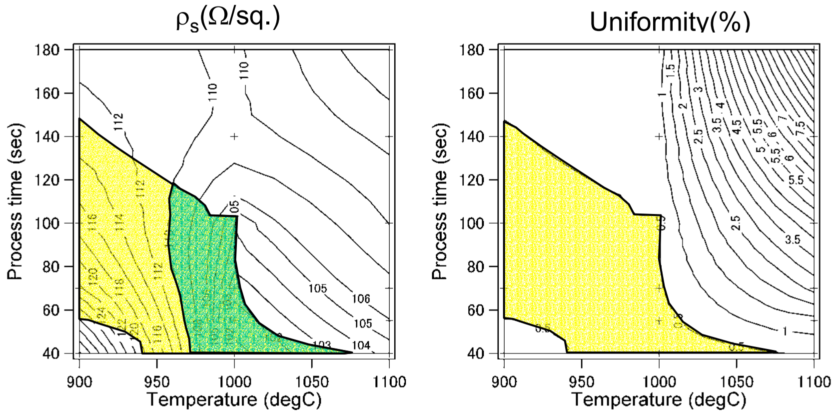
B^+ 50KeV, 1E15 atoms/cm^2

Sheet Resistance <90(Ω/sq.)



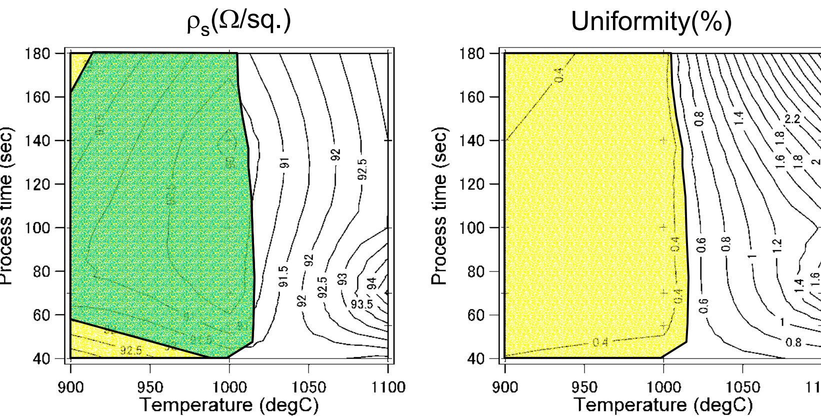
BF_2^+ 70KeV, 1E15 atoms/cm^2

Sheet Resistance <110(Ω/sq.)



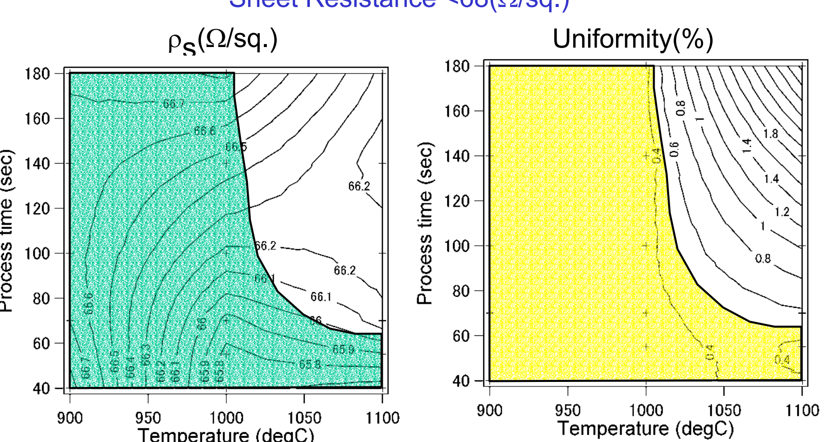
As^+ 70KeV, 1E15 atoms/cm^2

Sheet Resistance <92(Ω/sq.)



P^+ 70KeV, 1E15 atoms/cm^2

Sheet Resistance <68(Ω/sq.)

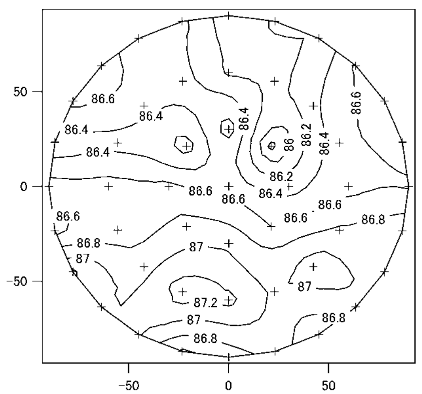


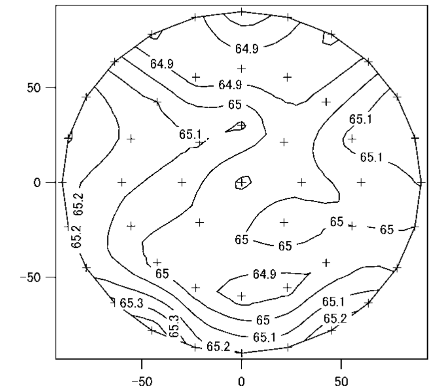
Typical Implant Anneal Process Uniformity

^{11}B 50keV 1E15

1100°C, 35s

Ave.= 86.63Ω/sq.
1σ= 0.95Ω/sq.
Unif.= 0.39%(1σ)





^{31}P 70keV 1E15

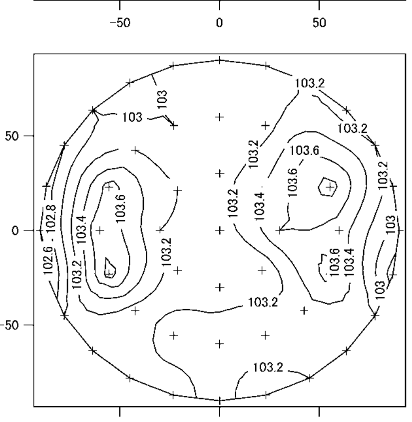
1000°C, 35s

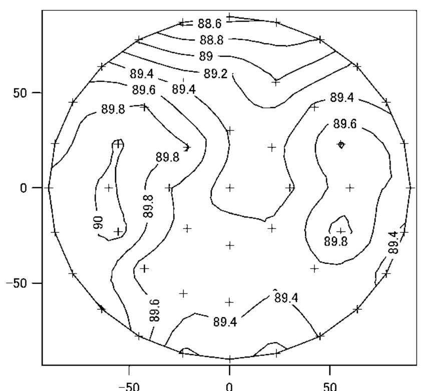
Ave.= 65.05Ω/sq.
1σ= 0.16Ω/sq.
Unif.= 0.25%(1σ)

BF_2 70keV 1E15

1000°C, 35s

Ave.=103.19Ω/sq.
1σ= 0.31Ω/sq.
Unif.= 0.30%(1σ)





^{75}As 70keV 1E15

1050°C, 35s

Ave.= 89.46Ω/sq.
1σ= 0.37Ω/sq.
Unif.= 0.41%(1σ)

Implant Anneal Summary

$^{75}As^+$ 70keV 1E15
$^{31}P^+$ 70keV 1E15
$^{49}BF_2^+$ 70keV 1E15
$^{11}B^+$ 50keV 1E15

SWF 40s

$^{11}B^+$
$^{49}BF_2^+$
$^{75}As^+$
$^{31}P^+$

Sheet Resistance (Ohm/sq.)
300
250
200
150
100
50
850 900 950 1000 1050 1100 1150
Temperature (°C)

Lamp RTP 10s

$^{11}B^+$
$^{49}BF_2^+$
$^{75}As^+$
$^{31}P^+$

Sheet Resistance (Ohm/sq.)
300
250
200
150
100
50
850 900 950 1000 1050 1100 1150
Temperature (°C)

Rs Uniformity (%)
12.0
10.0
8.0
6.0
4.0
2.0
0.0
850 900 950 1000 1050 1100 1150
Temperature (°C)

Rs Uniformity (%)
12.0
10.0
8.0
6.0
4.0
2.0
0.0
850 900 950 1000 1050 1100 1150
Temperature (°C)

$^{11}B^+$ Implant Anneal

$^{11}B^+$ 50keV, 1E15 cm^{-2}

As implanted

900°C
10s 236.78 Ω/sq.
150s 158.39 Ω/sq.

1000°C
10s 101.14 Ω/sq.
70s 88.58 Ω/sq.
150s 86.70 Ω/sq.

1100°C
10s 86.92 Ω/sq.
70s 87.79 Ω/sq.
150s 90.22 Ω/sq.

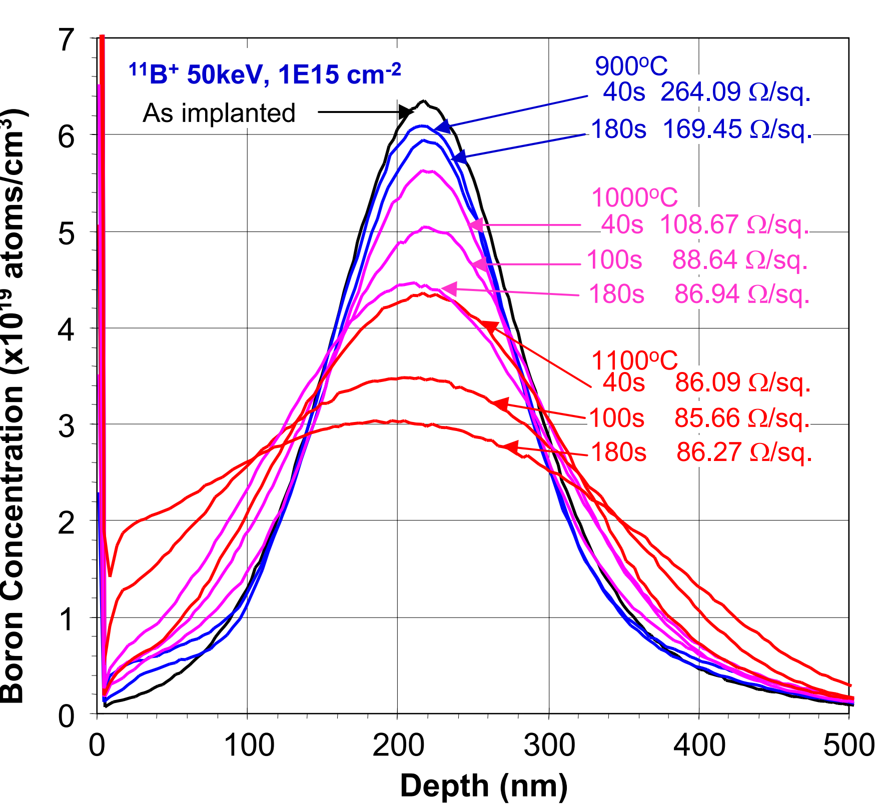
Boron Concentration (x10^{19} atoms/cm^3)

Depth (nm)

0 1 2 3 4 5 6 7

0 100 200 300 400 500

SWF

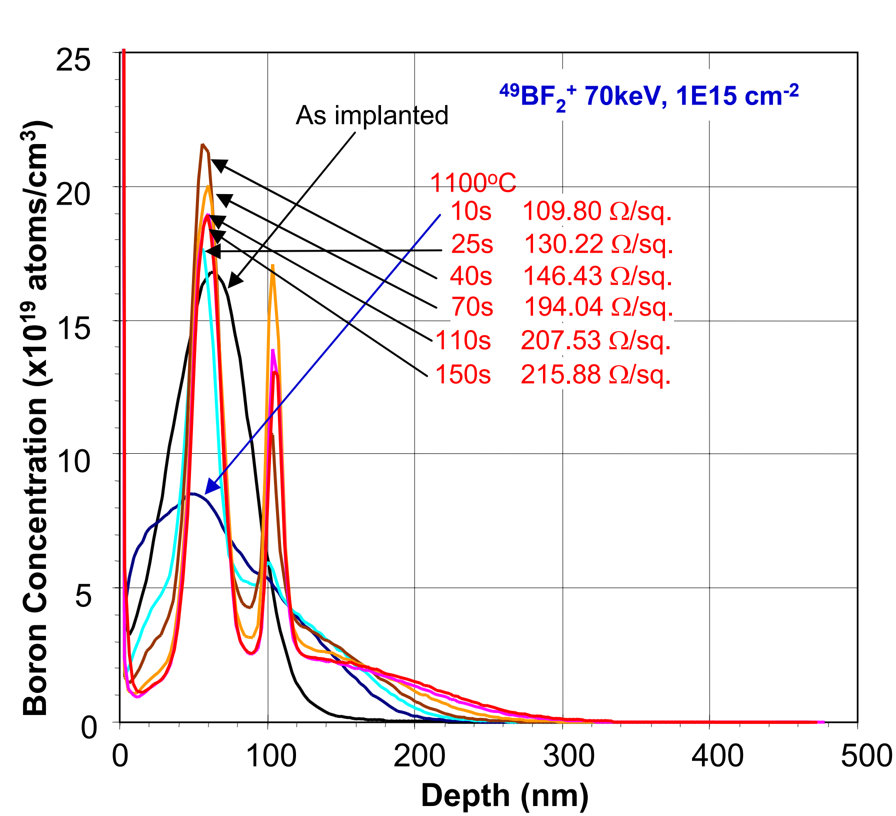


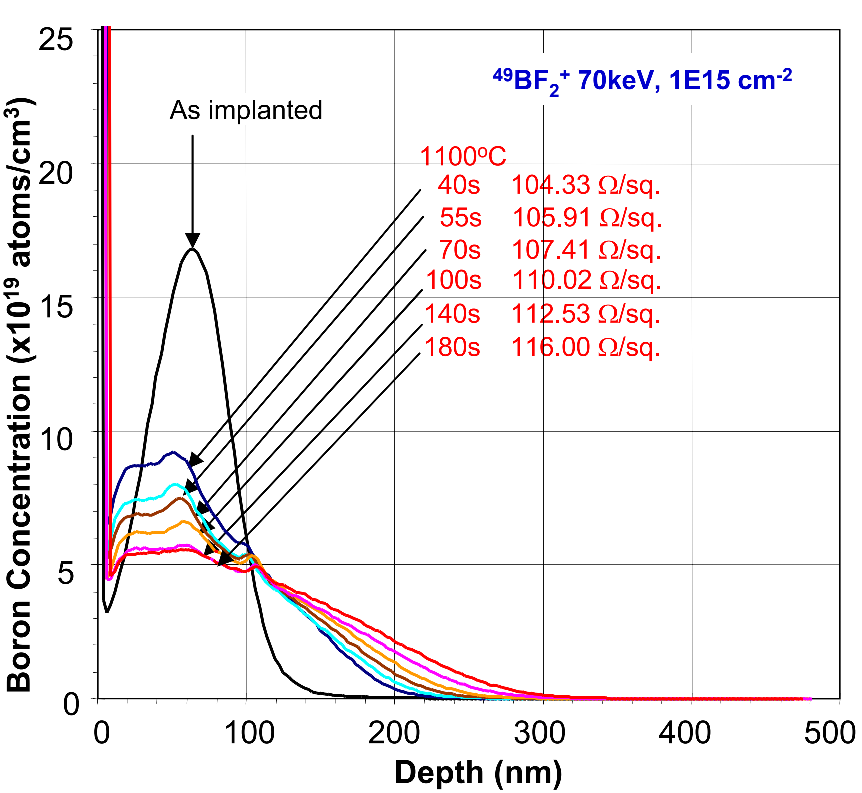
$^{49}BF_2^+$ Implant Anneal

1100°C

Lamp RTP

SWF





BPSG Film Densification/Reflow

Thickness Shrinkage (%)

5.0
4.0
3.0
2.0
1.0
0.0

1000ºC
950ºC
900ºC
850ºC
800ºC
750ºC
700ºC
650ºC
600ºC

Δ Unif. (%)

0.5
0.0
-0.5

0
50
100
150
200

Annealing Time (s)

Maximum density reached with highest shrinkage

Titanium Silicide Formation and Anneal

700 Torr, N_2 Atmosphere, Ti = 35nm

Post Rs (Ohm/sq.)

70
60
50
40
30
20
10
0

500 600 700 800 900 1000

Temperature (°C)

60s
90s
120s

Rs Change Ratio

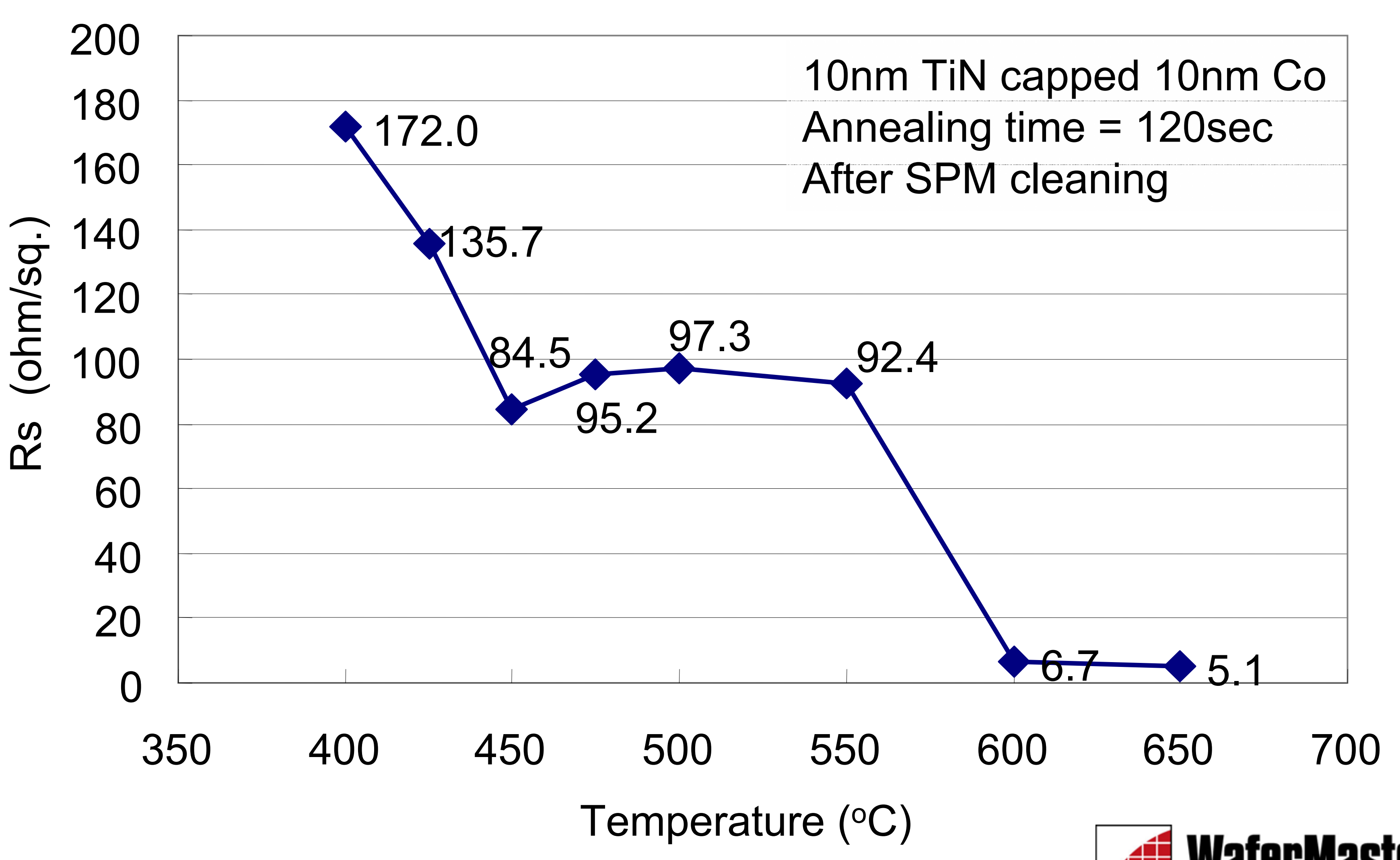
3
2.5
2
1.5
1
0.5
0

500 600 700 800 900 1000

Temperature (°C)

60s
90s
120s

Temperature Sensitivity for CoSi Formation



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Co_xSi Formation (10nm TiN capped 10nm Co)

Process conditions : 425°C, 150sec, After SPM cleaning

Slot #01

Slot #15

Slot #23

Average : 74.2 ohm/sq
Maximum : 77.4 ohm/sq
Minimum : 70.6 ohm/sq
Uniformity : 2.25%

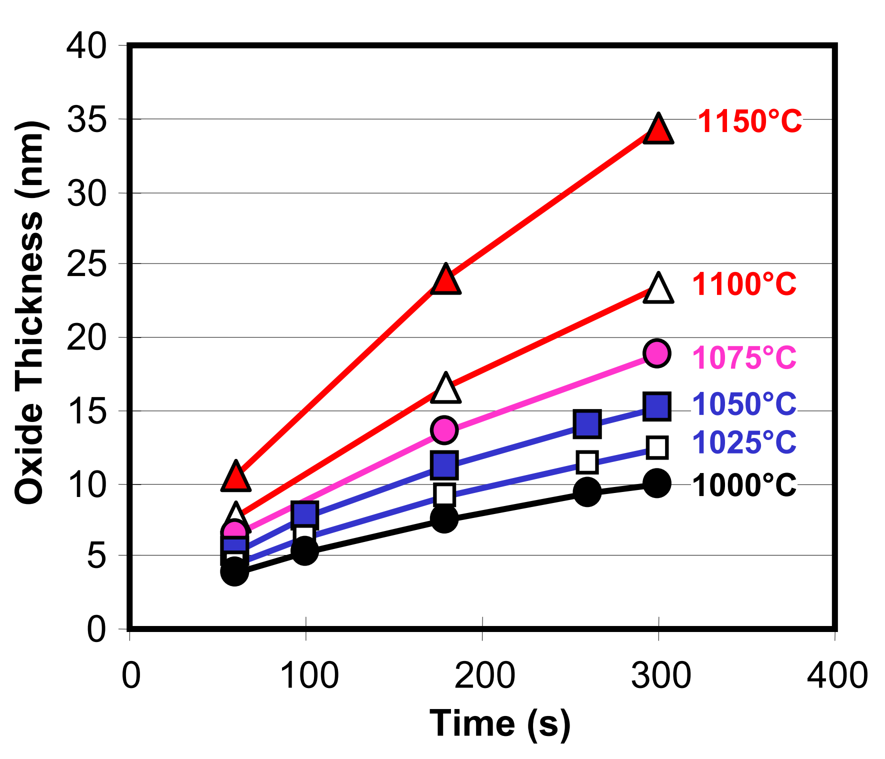
Average : 73.6 ohm/sq
Maximum : 79.2 ohm/sq
Minimum : 69.0 ohm/sq
Uniformity : 2.28%

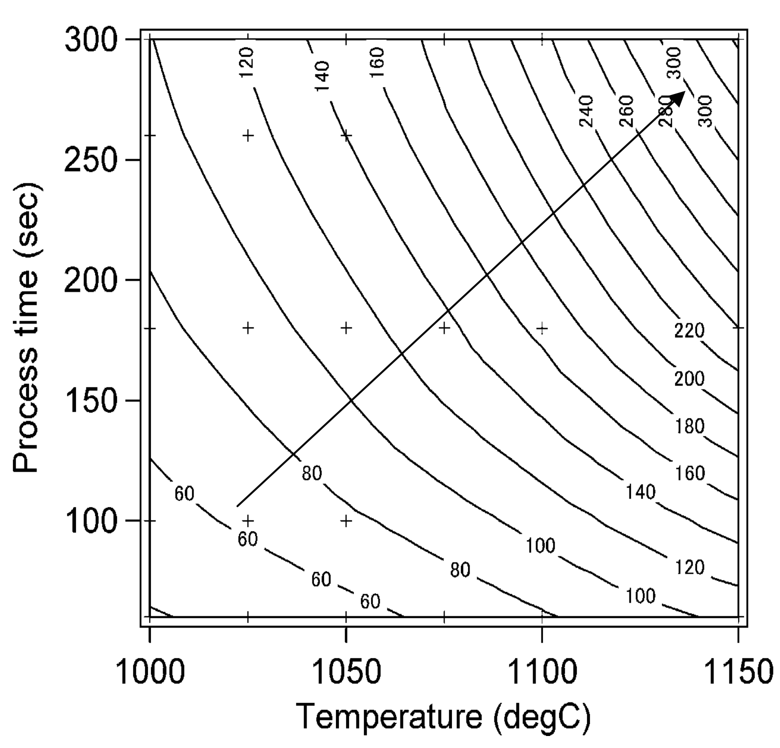
Average : 73.2 ohm/sq
Maximum : 79.0 ohm/sq
Minimum : 69.3 ohm/sq
Uniformity : 2.62%

Wafer to Wafer Repeatability (Max-Min)/2Ave =±0.68%

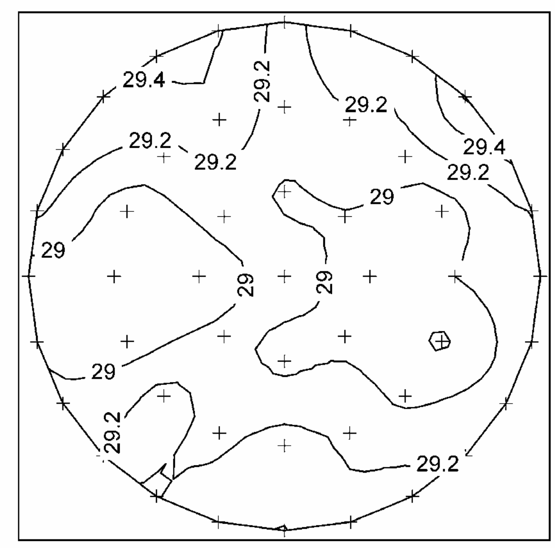
Oxide Thickness vs. Oxidation Time

O_2=0.5SLM, 760Torr

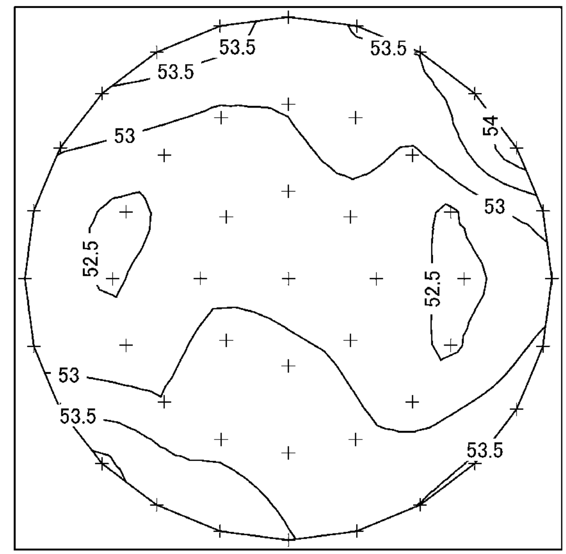




Typical Thin Dry Oxide Films



1000°C, 100s, 760Torr
O_2=0.3slm, N_2 = 2.7slm
Average = 2.9nm, Unif.= 0.67%



1000°C, 100s, 760Torr
O_2=0.5slm, N_2 = 0slm
Average = 5.3nm, Unif.= 0.91%

1000 Wafer Marathon Run

Thickness
Uniformity

1000°C, 100s
O_2 = 0.5slm, 760Torr

Average Oxide Thickness (nm)

6.0
5.5
5.0
4.5
4.0
3.5
3.0

Thickness Uniformity (%)

6.0
5.0
4.0
3.0
2.0
1.0
0.0

1 250 500 750 1000

Run Number

- **Extremely Repeatable**
  - Thickness: 0.8% (1σ)
  - Uniformity

Wafer Temperature Ramp Up Profile

Standoff Height

8 mm

He

Air

450
400
350
300
250
200
150
100
50
0

Wafer Temperature (ºC)

0 60 120 180 240 300

Time (s)

Hot Plate

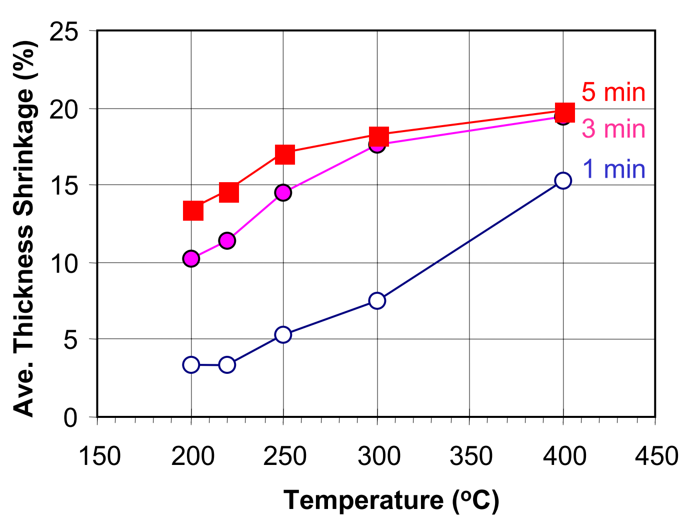
Wafer

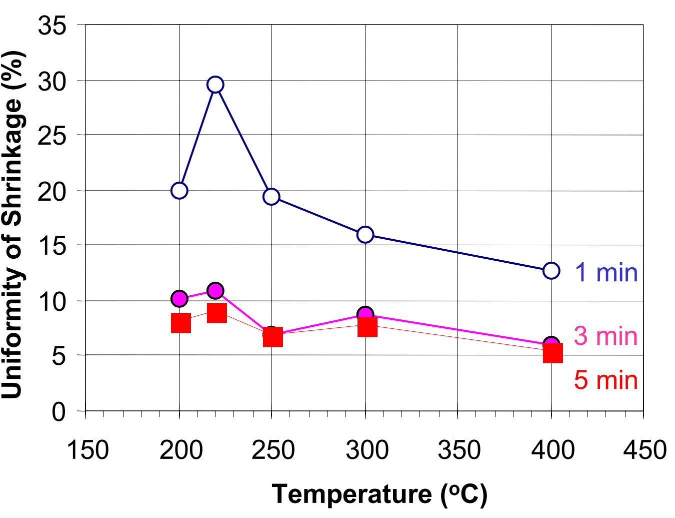
Heater

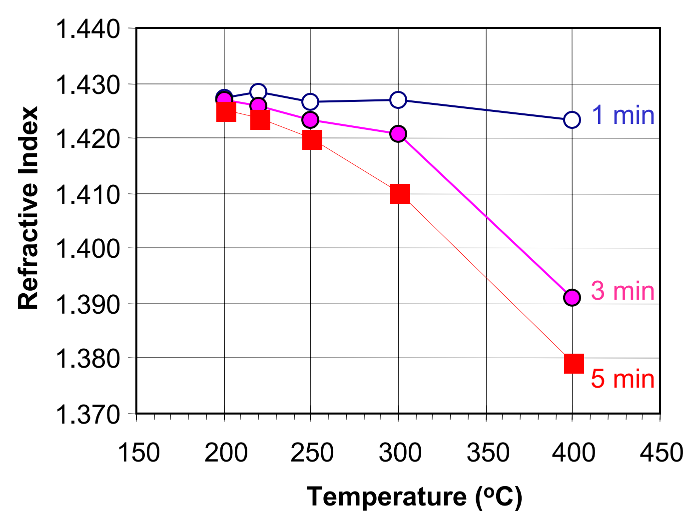
Hot Plate

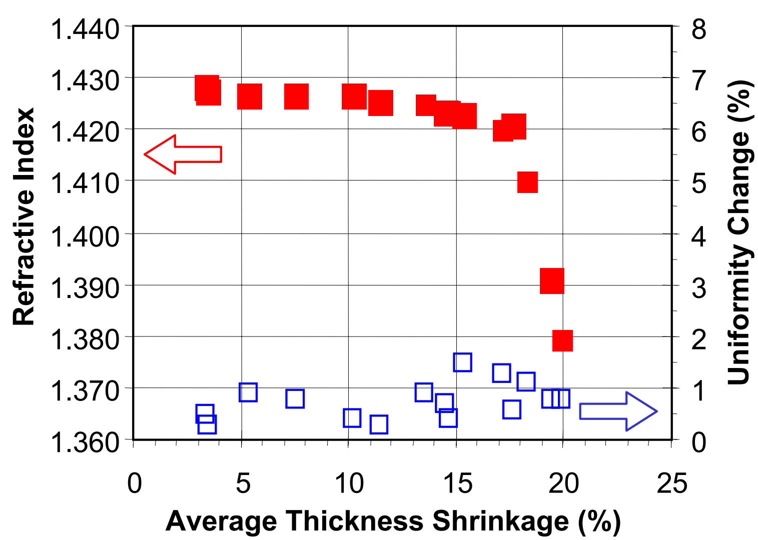
Standoffs

SOG Anneal Process Trends

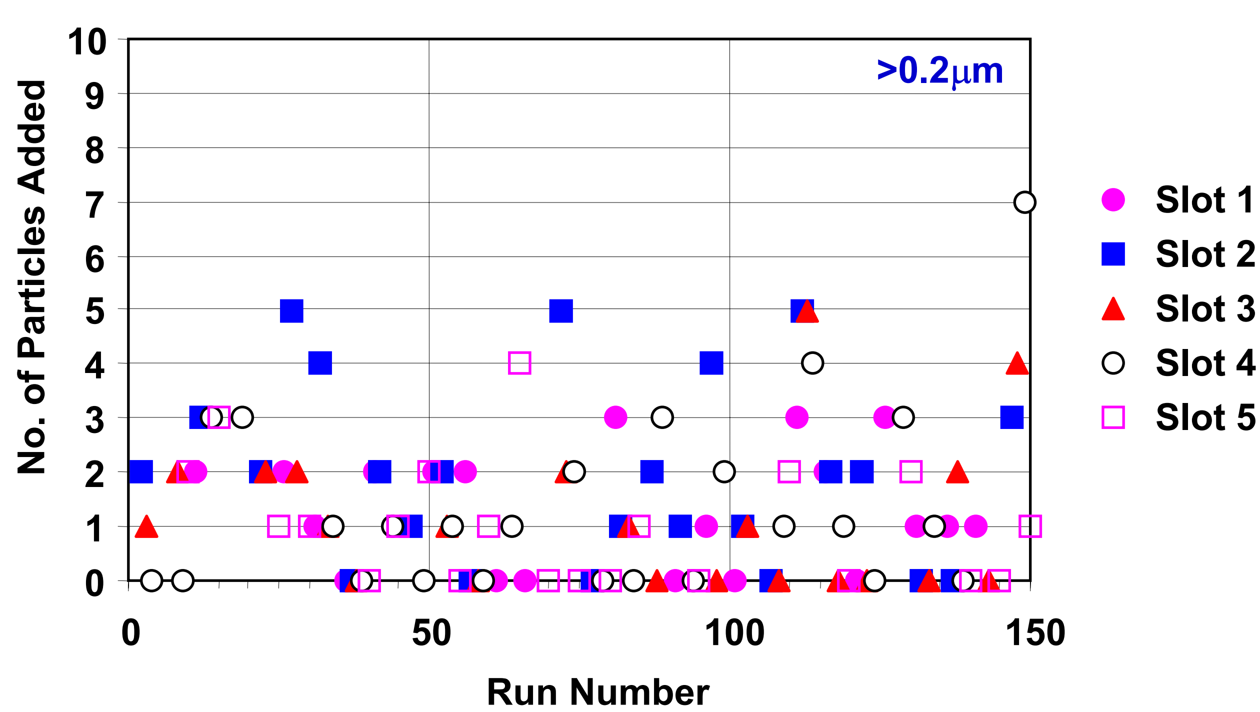








Particle Performance



Stacked Annealing Oven (SAO-200LP)

for Cu, NiSi and low K Dielectrics Applications

Process Module
- Stacked Hot Plates

Load Port
- Triangular door

Optical Bench
- No adjustment

Vacuum Robot
- Extended z-axis travel

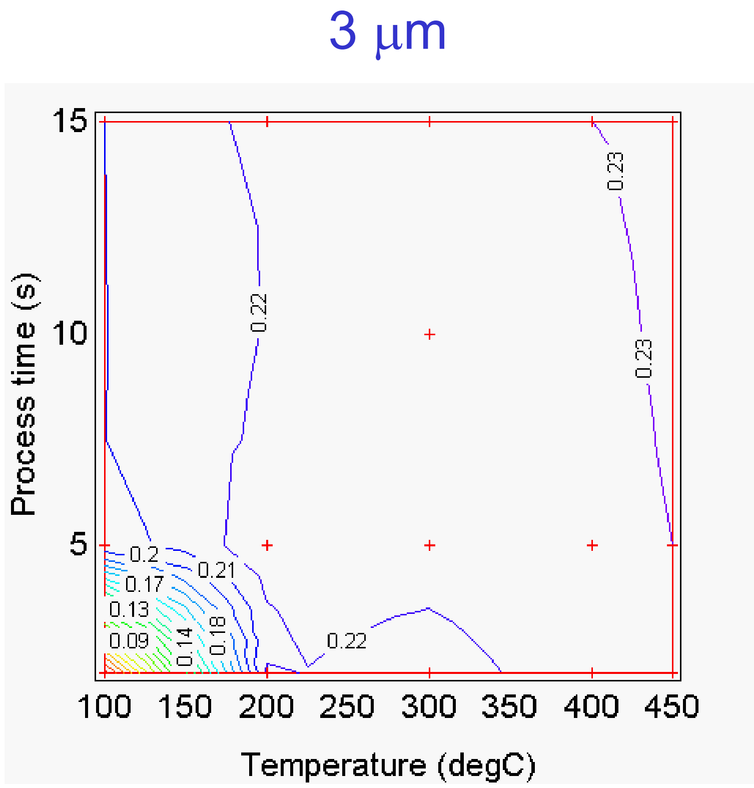
Cassette Stage
- Cooling stations

Vacuum Pump
- Integrated

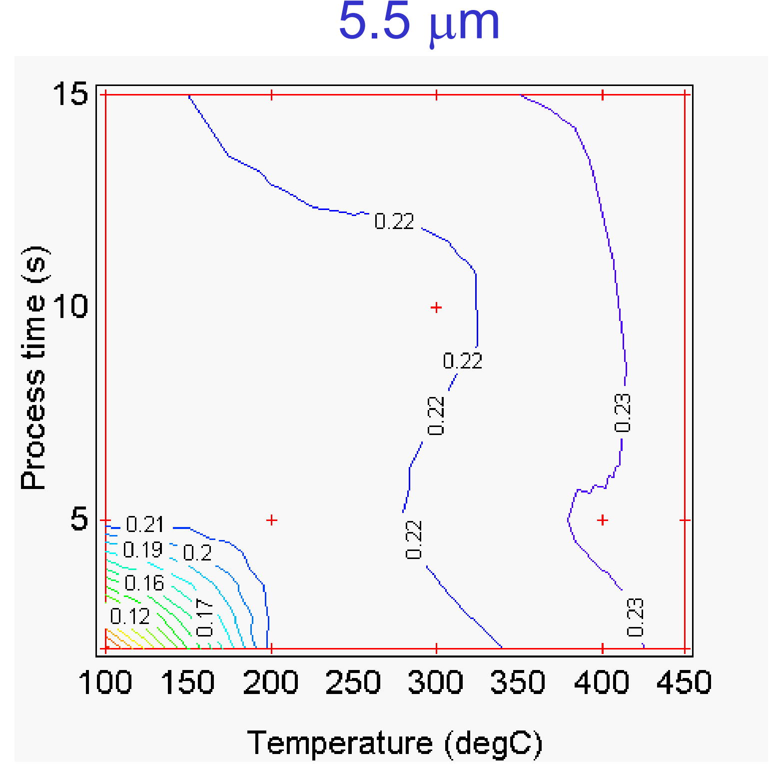
Surface Response of Rs Reduction Ratio

Cu Anneal in Forming Gas

3 μm



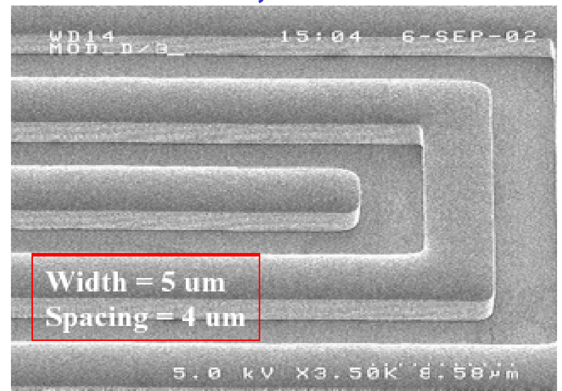
5.5 μm

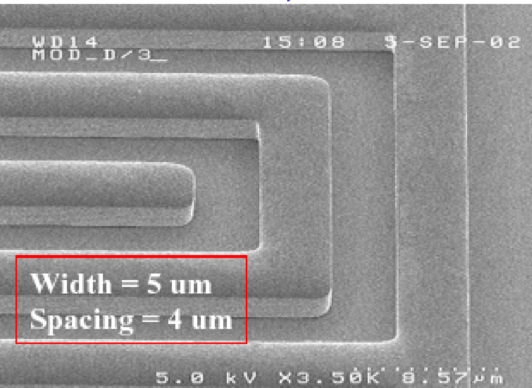


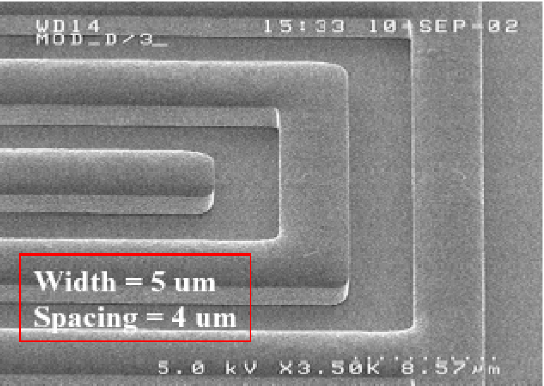
Cu Grain Growth by Annealing

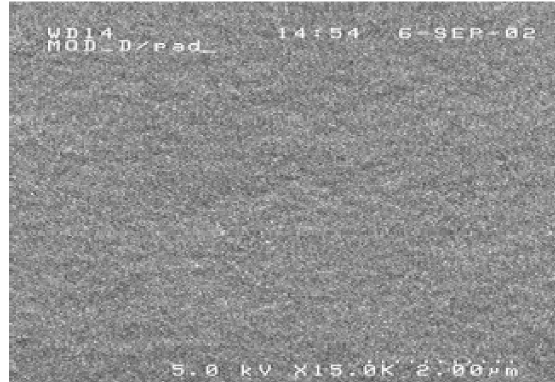
Cu Thickness = 3.0 μm
1 atm forming gas

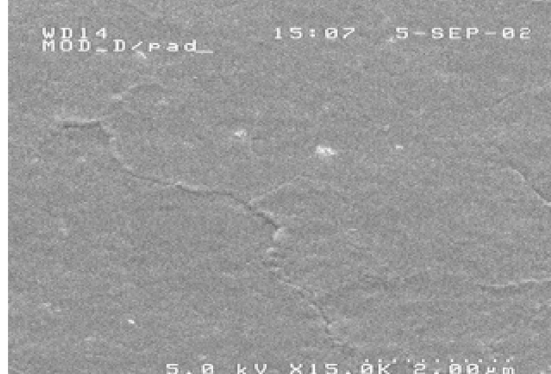
200°C, 5 min | **300°C, 5 min** | **400°C, 5 min**

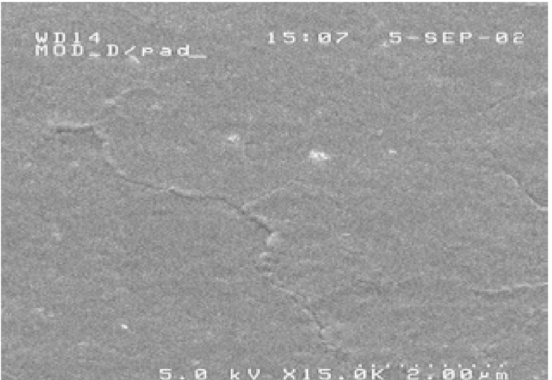












NiSi Sheet Resistance Changes between Pre and Post-annealing

239Ω/sq
238Ω/sq

SAO
SRTF

SRTF-pre
SRTF-post
SAO-pre
SAO-post

Sheet Resistance (Ω/sq)
0 10 20 30 40 50

200 300 400 500 600 700
Heater temperature (°C)

-Silicidation in SAO was obtained at temperatures from 350°C to 550°C with TiN uncapped samples on as well as capped samples.

-Increasing sheet resistance was observed above 600°C, 650°C was already too high to form stable NiSi.

Reflectance Properties of NiSi

After Formation at Various Temperatures

Reflectance

0.7
0.6
0.5
0.4
0.3
0.2

200 300 400 500 600 700 800

Wavelength (nm)

Showed lowered Rs

SAO 250C
SAO 300C
SAO 350C
SAO 450C
SAO 550C
SRTF 600C
SRTF 650C
SRTF 700C

-Reflectance indicates film transformation confirmed by sheet resistance changes.

Surface Roughness - AFM Image

TiN/Ni(90A)/Si-sub

SAO-Capped		
$200^{o}C \rightarrow 450^{o}C$	$250^{o}C \rightarrow 450^{o}C$	$450^{o}C$
3.0nm	3.0nm	3.0nm
Rs= 8.0 Ω/sq. Unif.= 4.59 %	Rs= 8.0 Ω/sq. Unif.= 4.66 %	Rs= 8.7 Ω/sq. Unif.= 5.01 %
Ra= 0.142 nm Rz= 1.284 nm	Ra= 0.129 nm Rz= 1.187 nm	Ra= 0.130 nm Rz= 1.207 nm

Flash Anneal System Concept

- Motivation : USJ formation (Shallow implantation is a must!)
  - Maximum electrical activation
  - Least amount of diffusion
- Light Source : Short wavelength, high intensity light pulse
  - Xe arc lamp
  - Photon energy distribution
- Wafer Temperature : Mainly surface heating
  - Surface vs. Bulk
  - Time dependence

Spectral Emission of Lamps

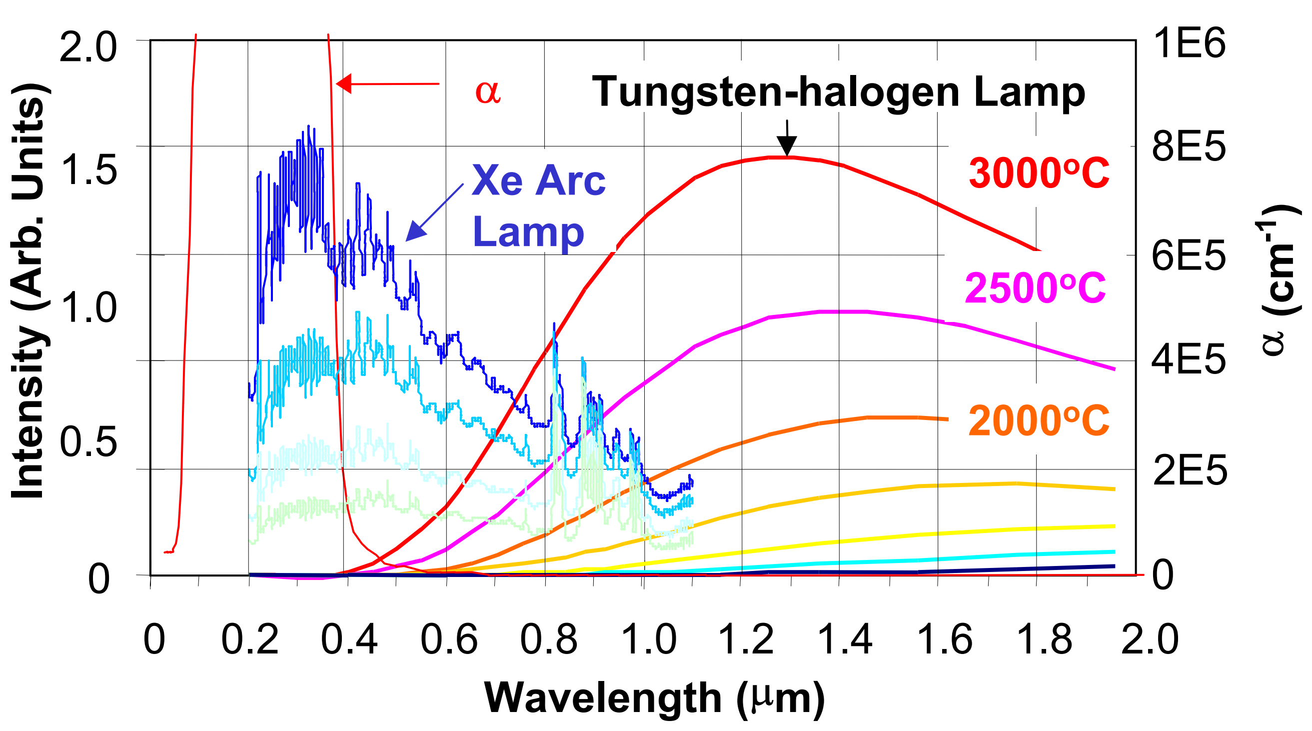
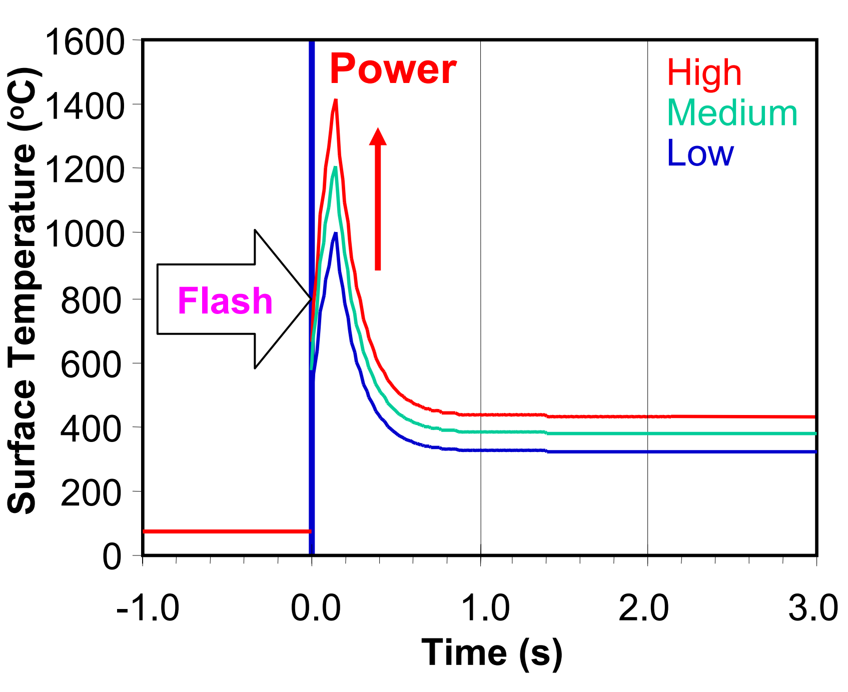
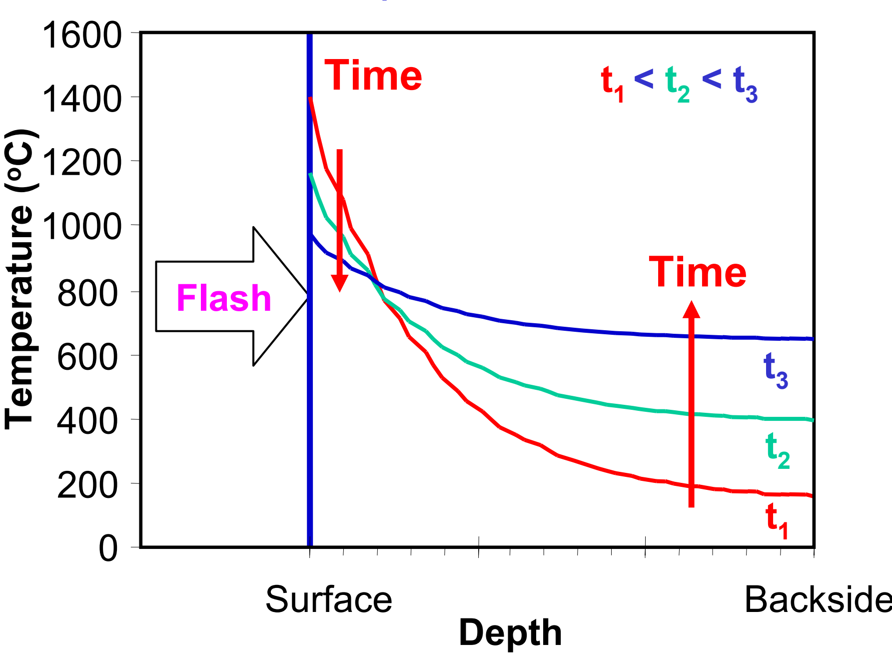


Illustration of Wafer Temperature Profile

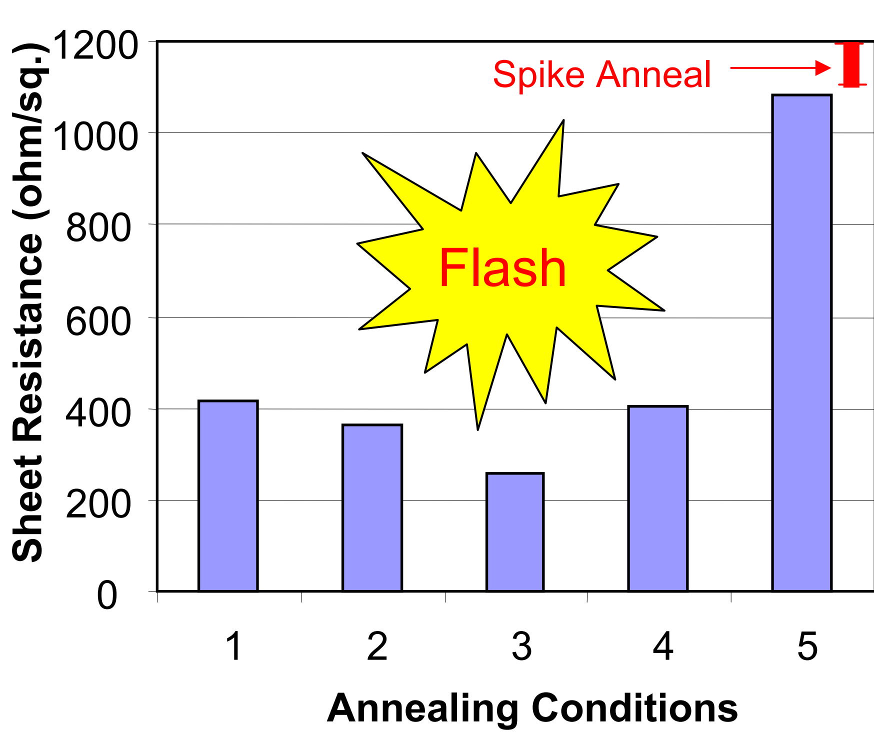


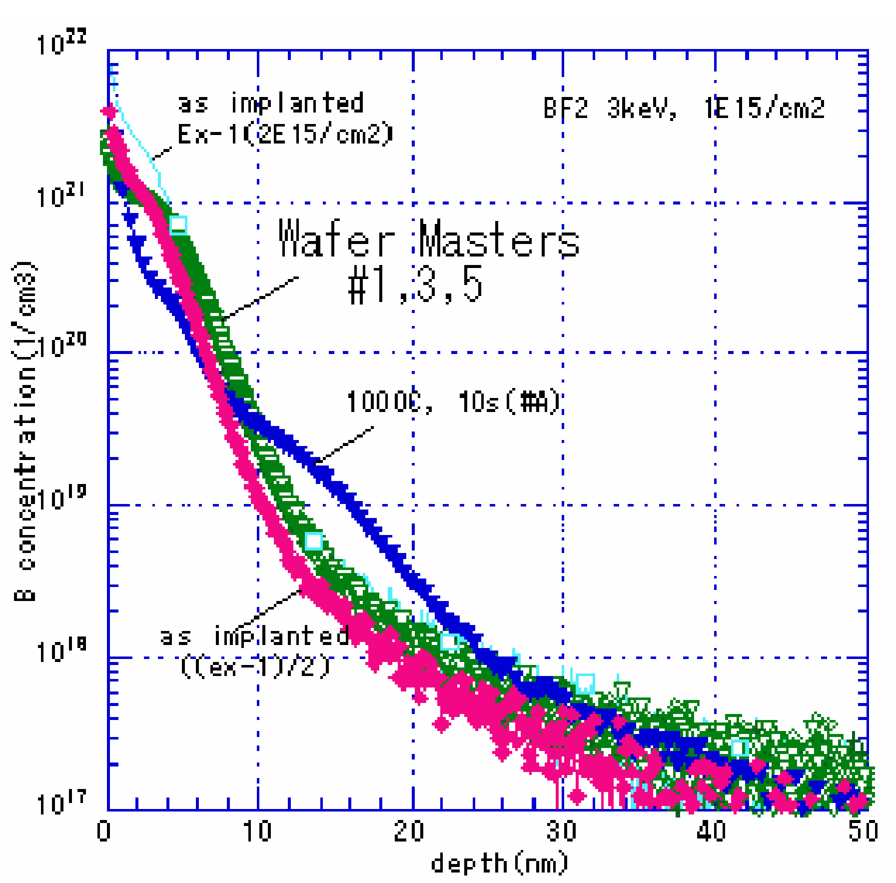
Bulk Temperature vs. Time



USJ Implant Anneal

$^{49}BF_2^+$, 3keV, 1 x10^{15}cm^{-2}





Implant Species: $^{49}BF_2^+$

Implant Energy: 3keV

Implant Dose: 1.0x10^{15}cm^{-2}

Surface Condition: 1.0~1.5nm Chemical SiO_2

Amorphorized Layer Thickness: ~10nm

USJ Implant Anneal

$^{11}B^+$, $^{49}BF_2^+$ Various Implant and Annealing Conditions

Sheet Resistance (Ohm/sq.)

10000
1000
100
10

0 10 20 30 40 50 60 70 80 90 100

Junction Depth x_j (nm)

ITRS 2002
65 nm
70 nm
80 nm
90 nm
100 nm
130 nm

RTA { Crystalline / Pre-amorphized
Flash Combination

1.0×10^{19}
2.0×10^{19}
5.0×10^{19}
1.0×10^{20}
2.0×10^{20}

Carrier concentration (cm^{-3})

USJ Implant Anneal with Flash

$^{11}B^{+}$ 1keV 1 x 10^{15} cm^{-2}

Lamp Only (CW)

Hot Plate + Lamp

Summary

- Developed RTP technology based on natural characteristics of wafer
- Demonstrated equivalent processes for ion implant anneal as obtained with lamp based RTP
- System operation insensitive to emissivity characteristics of wafer and wafer surface
- Temperature operation over wide temperature range
- New FLASH technology for USJ demonstrated