Ultra-Shallow Junction Formation using Flash Annealing and Advanced Doping Techniques

J. Gelpey[1], S. McCoy1, A. Kontos[2], L. Godet[2], C. Hatem[2], D. Camm[1], J. Chan[1], G. Papasouliotis[2], J. Scheuer[2], P. Timans[1]
[1] Mattson Technology Inc.
[2] Varian Semiconductor Equipment Associates

West Coast Junction Technology Meeting
July 17, 2008

A Partner You Trust. Performance You Value.

Outline

- USJ requirements for sub-45nm nodes
- Advanced Doping Approaches for USJ formation
- Advanced Annealing Requirements for USJ
- Recent Process Results
- Summary and Conclusions

Shallow Junction Requirements

- ITRS Junction Roadmap
  - Calls for sub-10nm junction depth with sheet resistance values of ~1000Ω/sq. and abruptness of <2nm/decade

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*
Drain extension X_j (nm) for bulk MPU/ASIC [F]	**12.5**	**11**	**10**	**9**	**8**	**7**
Maximum allowable parasitic series resistance for bulk NMOS MPU/ASIC × width ((Ω?µm) from PIDS [G]	**200**	**200**	**200**	**180**	**180**	**180**
Maximum drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/sq) [G]	**650**	**740**	**810**	**900**	**1015**	**1160**
Extension lateral abruptness for bulk MPU/ASIC (nm/decade) [H]	**2.5**	**2.3**	**2.0**	**1.8**	**1.6**	**1.4**

Conventional junction technology cannot meet these goals

Additional Requirements

- Junction leakage is becoming a significant component of the overall device off-state leakage current and must be controlled
  - especially challenging for low power devices

- Traditional approaches for forming shallow junctions adversely impact junction leakage
  - Pre-amorphizing implants
  - Solid phase epitaxial regrowth for damage removal
  - Overall trend toward reduced anneal thermal budget

- To meet future junction requirements, doping and activation must be optimized as integrated process sequence

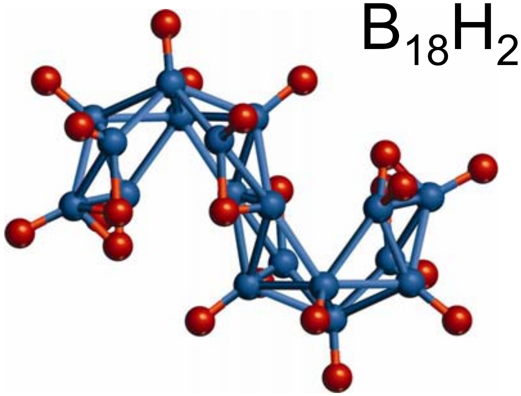
Advanced Doping Techniques

- Implantation challenges for USJ applications
  - Low productivity with monomer beamline implants at low energies
  - Energy contamination at low energies
  - Pre-amorphization to minimize channeling conflicts with low leakage requirement

- Novel doping techniques address these limitations
  - Plasma Doping ⇨high throughput
  - Large molecular species ($C_2B_{10}H_{12}$, $B_{18}H_{22}$)⇨high throughput, EC free, self amorphization
  - Advanced PAI schemes to reduce EOR and junction leakage

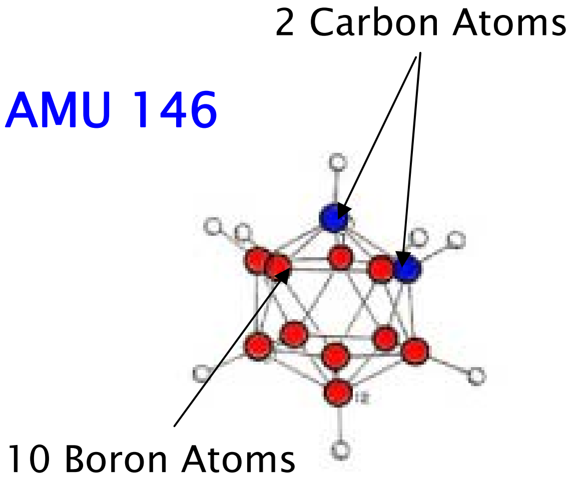
Molecular Implants

- **$B_{10}H_{14}$ & $B_{18}H_{22}$**:
  - Heavy molecules allow high throughput & Energy Contamination-free implants
- **<u>Carborane:</u>**
  - **Standard Source** – does not require a “soft” ionization approach
    - High thermal stability of molecule requires little change to ion source
      - Vaporizes at ~100°C
      - Stable to over 700°C
  - 10 dopant atoms per molecule
    - Extract and transport 13X voltage
    - Increased 10X effective dose rate
    - Decel not required: **EC Free Solution**
  - Uniform beams currents above 6mA demonstrated at 500eV equivalent
    - With upside for further increase
    - Uniform beams with angle spread <1.0º



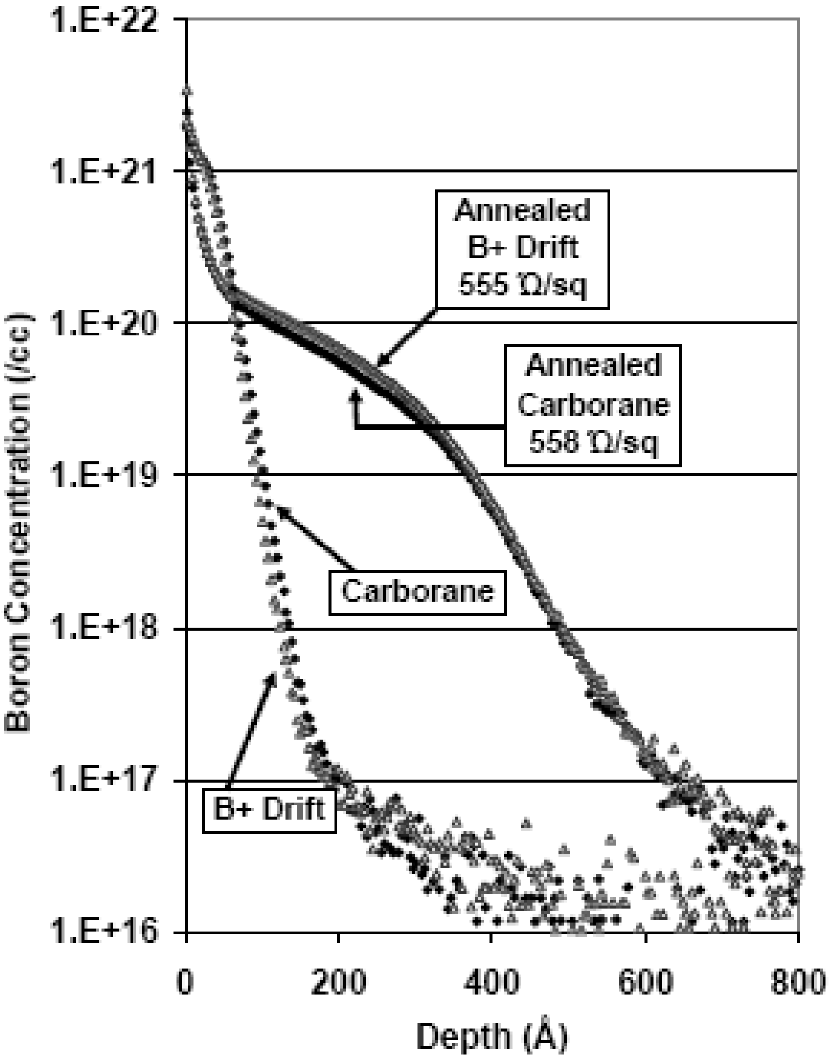
$B_{18}H_{22}$

Carborane ($C_2B_{10}H_{12}$)

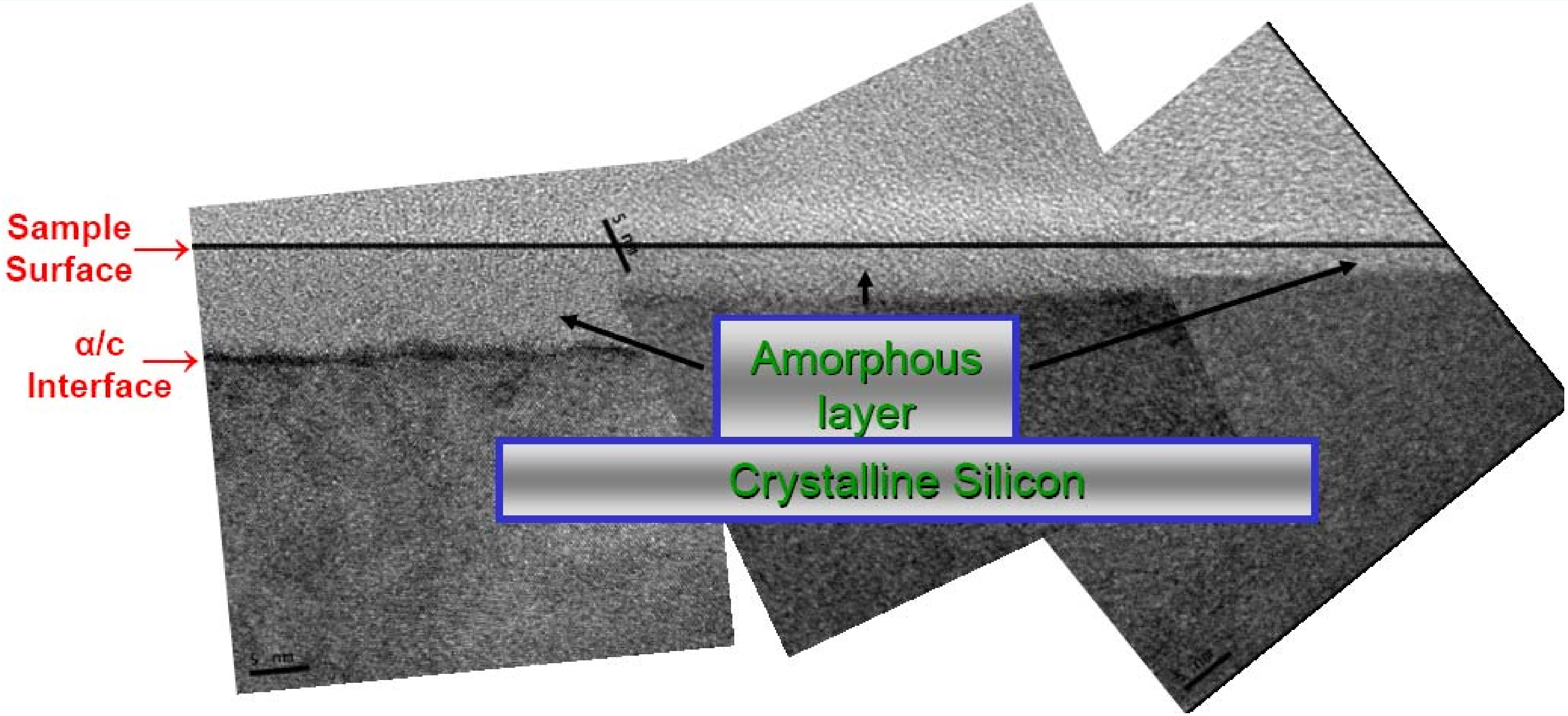


Carborane Molecular Implant Matches B^+

- Carborane SIMS profiles match those of 500eV B^+, before and after 1050°C spike anneal
- R_s also matches following 1050°C spike anneal



CBH Self Amorphization- XTEM As Implanted



CBH1.5keV
$1e15cm^{-2}$

α-layer ~70-75Å

CBH500eV
$1e15cm^{-2}$

α-layer ~35-40Å

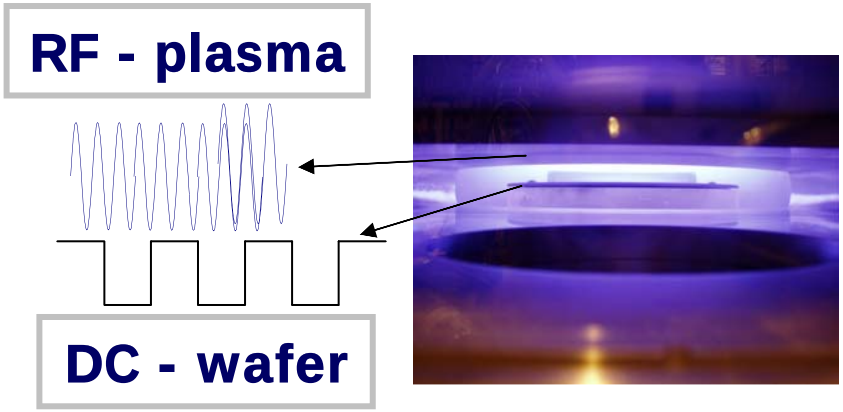
CBH200eV
$1e15cm^{-2}$

α-layer ~20-25Å

Ge^+12kev $3e14cm^{-2}$ amorphous depth ~185-190Å

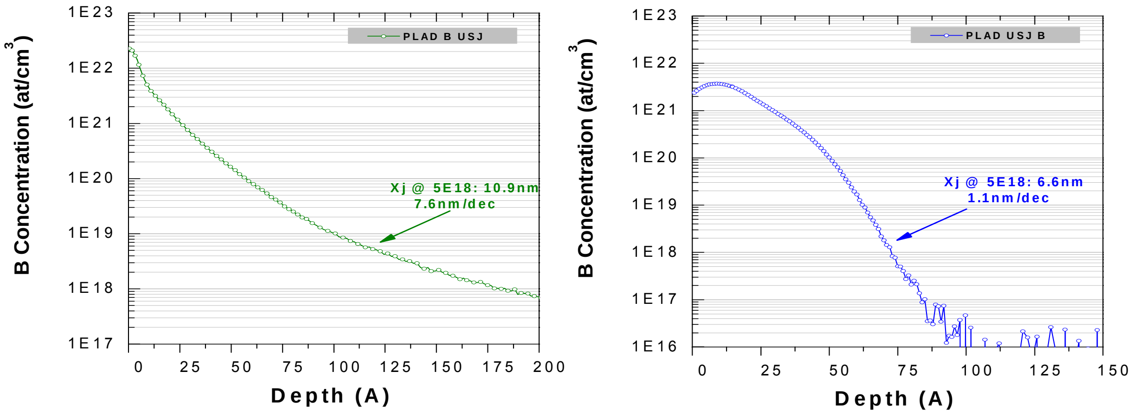
VIISta PLAD Key Technologies

- Highest Throughput
  - High density, Low energy RF plasma
    - ☐ High dose rate
    - ☐ Control over etch and deposition
- Precise Energy Control
  - Pulsed DC Wafer Bias
  - Wide energy range: 0.1 to 10kV
  - Rapid <1μs pulse rise and fall times
- Process Security
  - Real Time, in-situ dose control: Close Loop Faraday
  - Plasma Detector: Photocell
  - Good Metals performance: liner



RF - plasma

DC - wafer



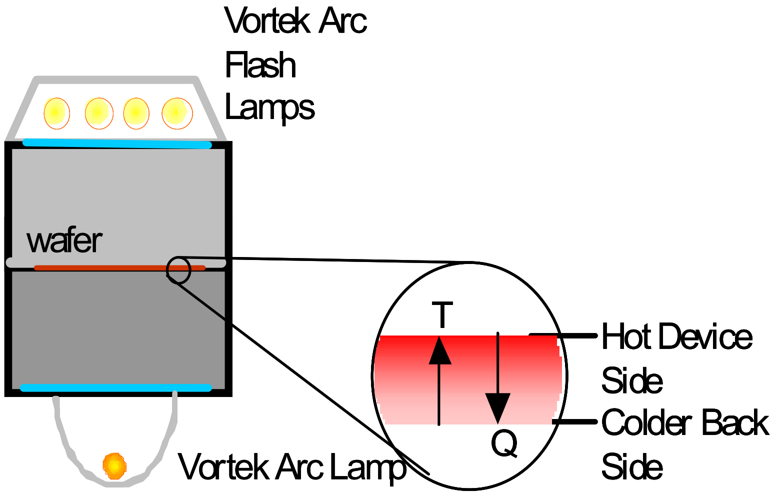
- As-Implanted Boron SIMS profiles

Advanced Annealing

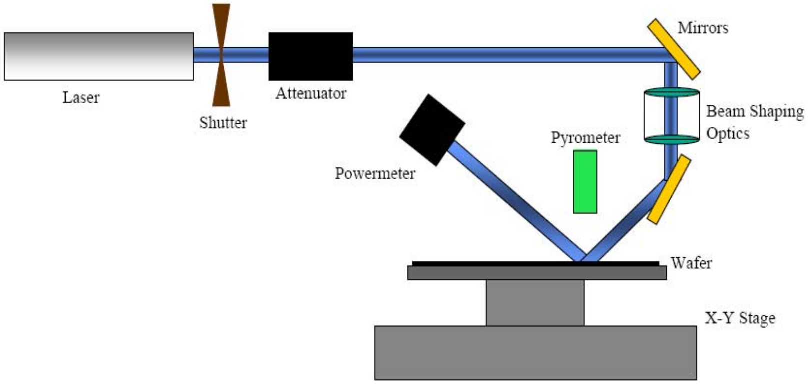
- Spike RTP annealing has been the standard for forming USJs
  - Effective annealing times (T_{peak}-50K) of about 1.5s
  - Difficult to reduce times due to thermal mass of tungsten-halogen lamps and the limitations of cooling rates
- Melt laser annealing with pulsed laser of ns-µs dwell times have been used, but have proven very difficult to integrate successfully
- Flash lamp or scanned CW sub-melt laser annealing with effective anneal times on the order of 10^{-4} to 10^{-2} seconds have recently become available (millisecond anneal or “MSA”)
  - Pulse duration is less than the thermal diffusion time constant of the wafer, thus only the top surface layer of the wafer is heated. The bulk of the wafer sinks the heat from the front enabling fast ramp down times.

Milli-second Annealing

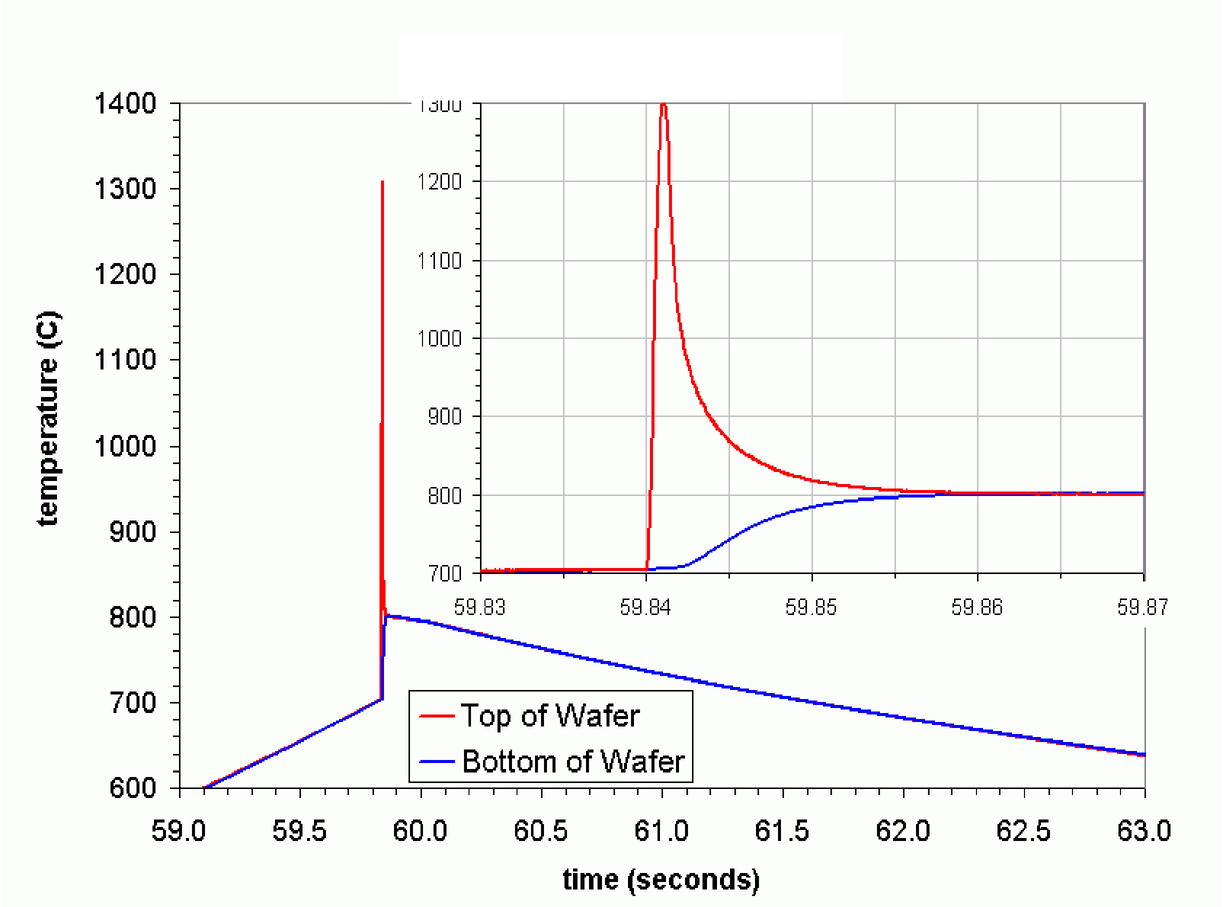
- Schematic of an example of the flash lamp MSA tool



- Schematic of a sub-melt laser MSA tool



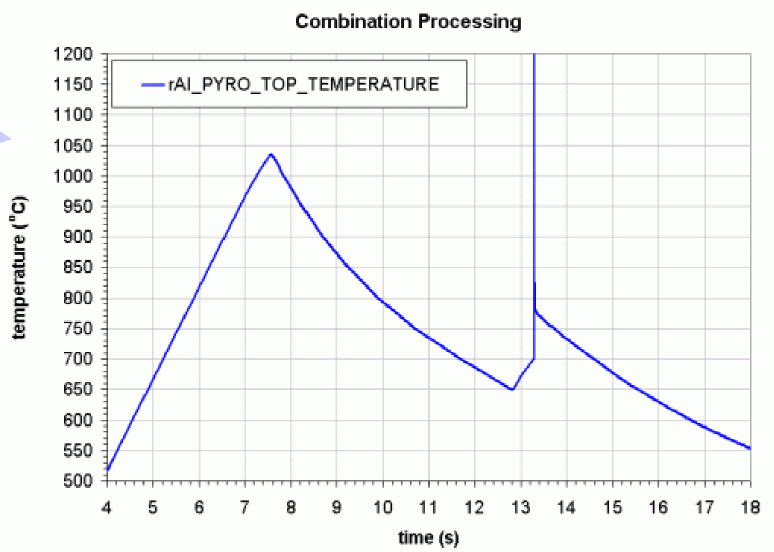
Temperature Profile of MSA

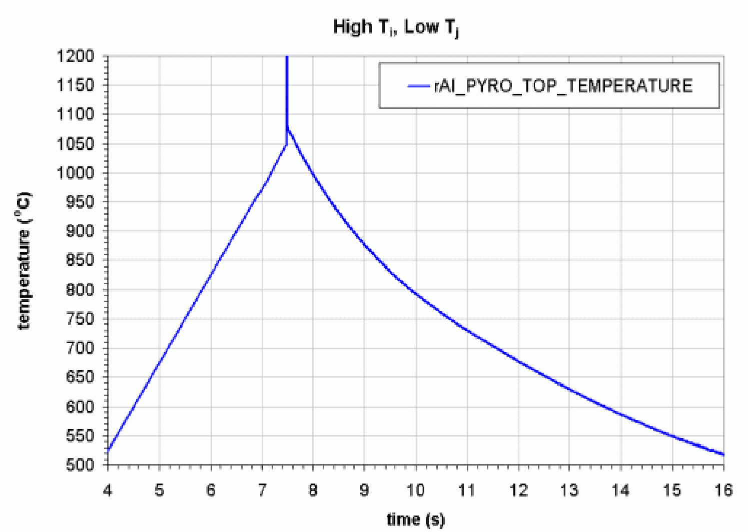


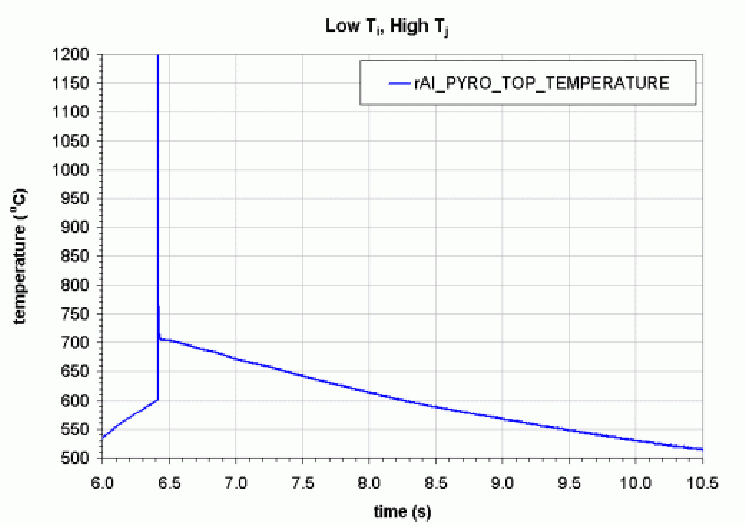
T_{peak}-50K of approx. 0.8ms. This example shows bulk heating using lamps.

Anneal Process Flexibility

Novel combination processes can be run to combine spike + flash

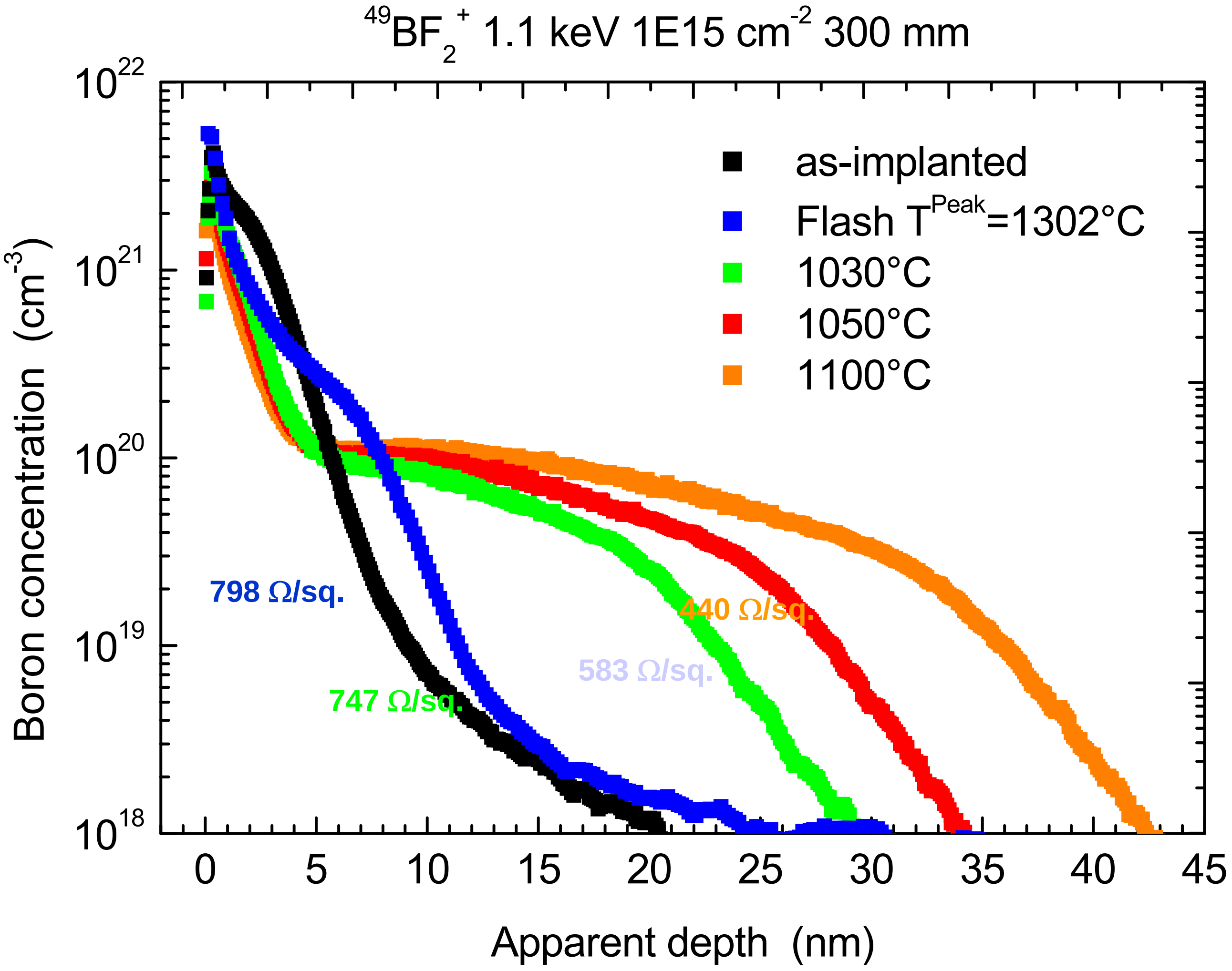






Unmatched process flexibility

Comparison FLASH to Spike for BF_2

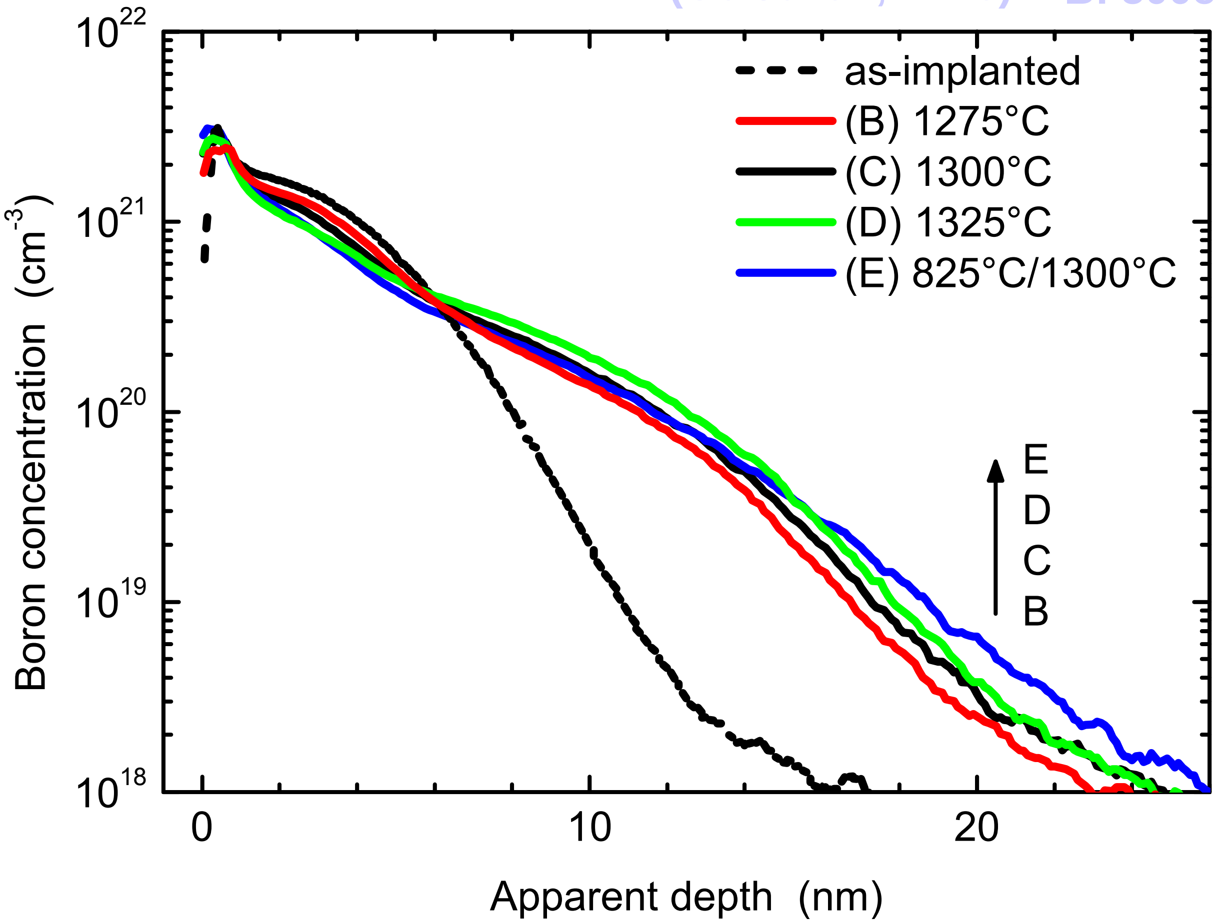


Ultra shallow junction - FLASH-annealed BF_2 implanted wafers

Effects of Variation of fRTP Peak Temperature

B in Ge pre-amorphized Silicon

(Ge 30keV, 1E15) B: 500eV, 1E15

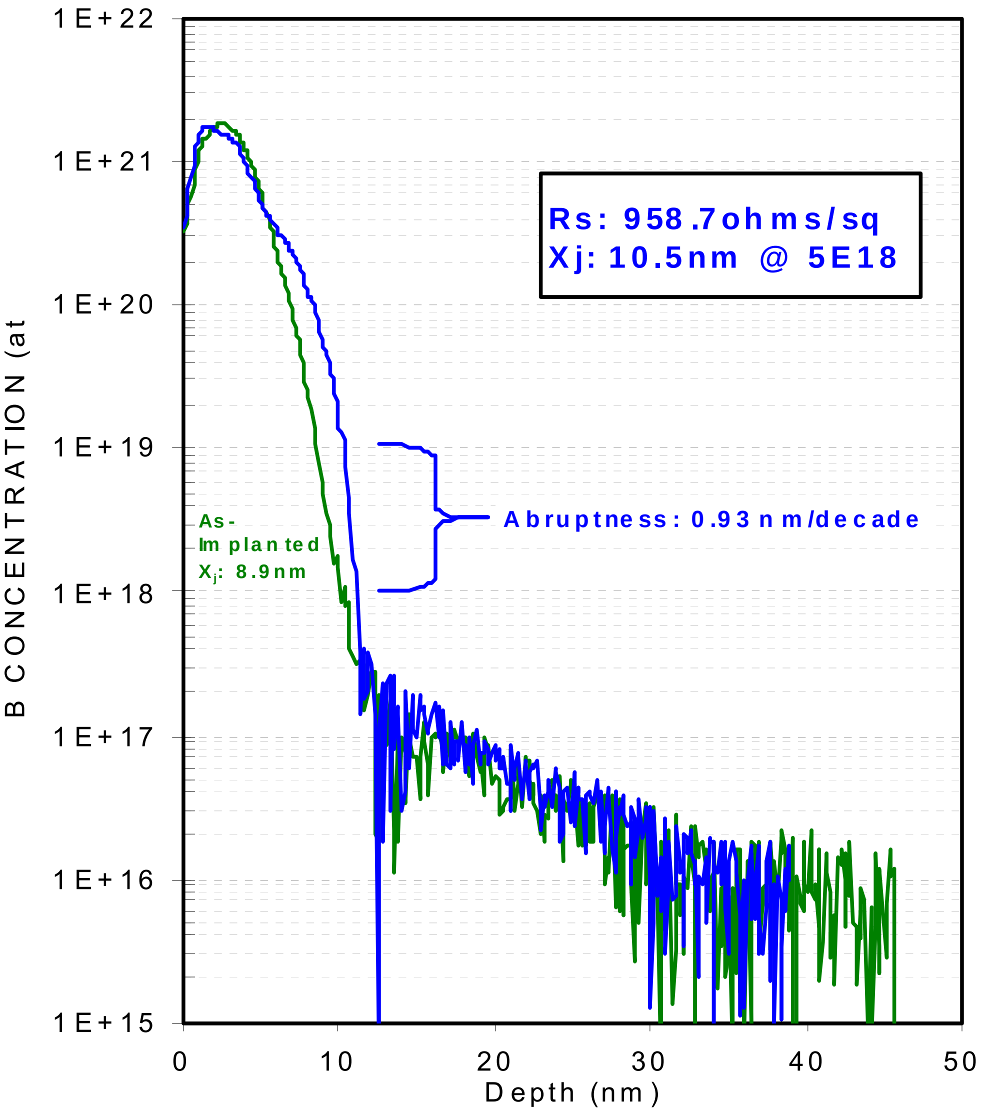


462 Ω/sq., 423 Ω/sq., 368 Ω/sq., 443 Ω/sq.

Diffusionless process increases electrically active dose

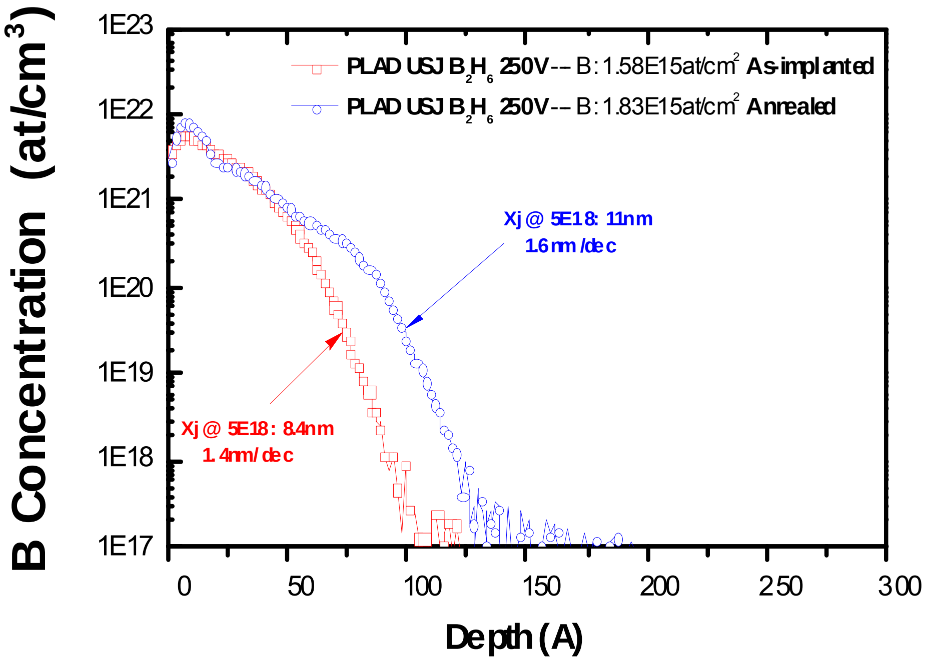
Boron Doping Profile:

Carborane Implant and MSA

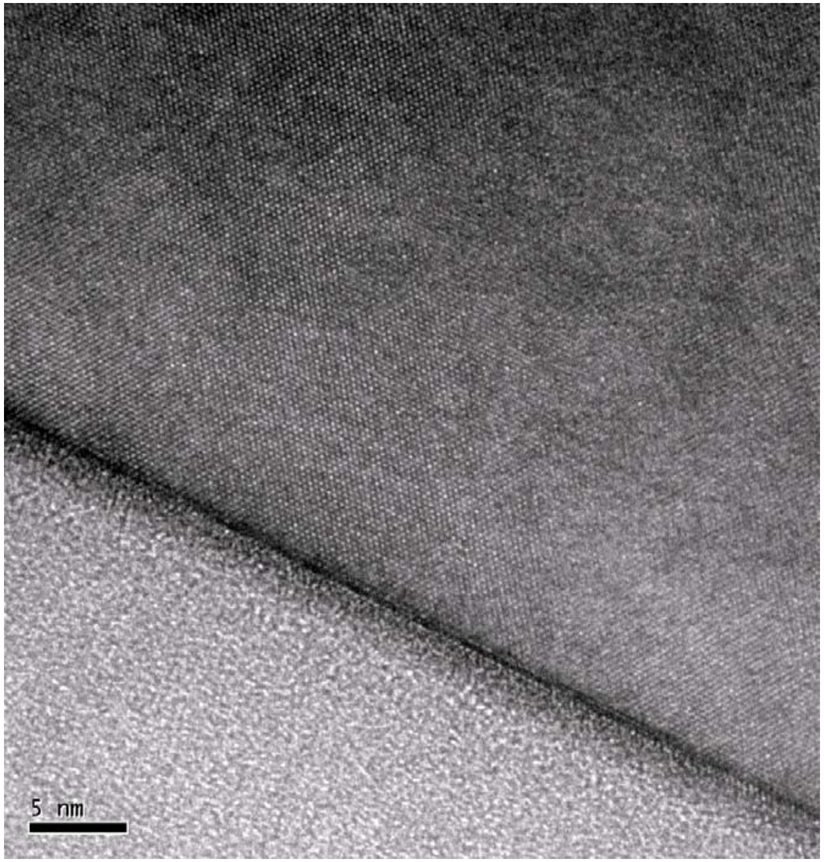


SIMS profile of flash annealed carborane implant. Note superior X_j/R_s and junction abruptness

Doping Profile using PLAD and FLA

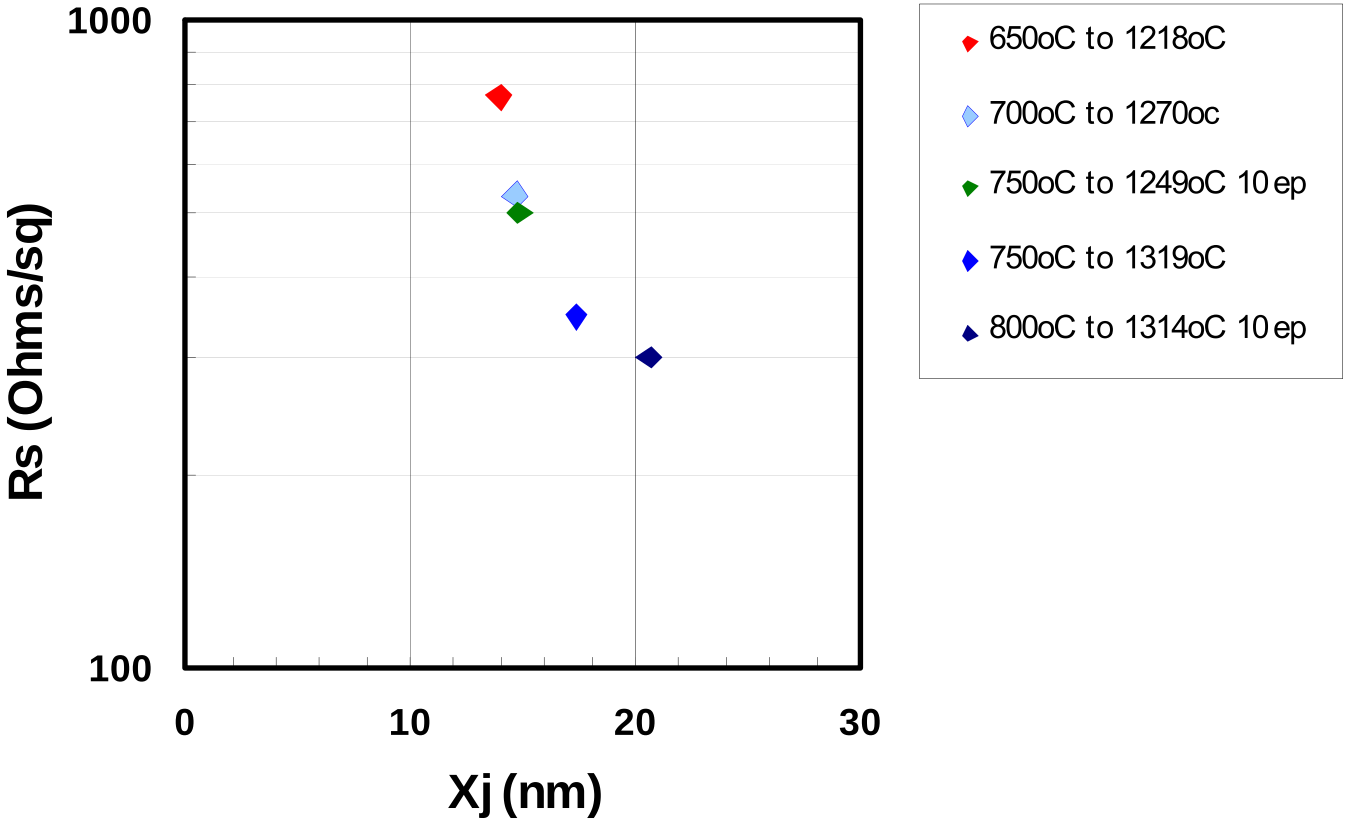


SIMS profile of PLAD implanted wafers annealed with fRTP. R_s/X_j is 11nm/820 Ω/sq. (@5E18).



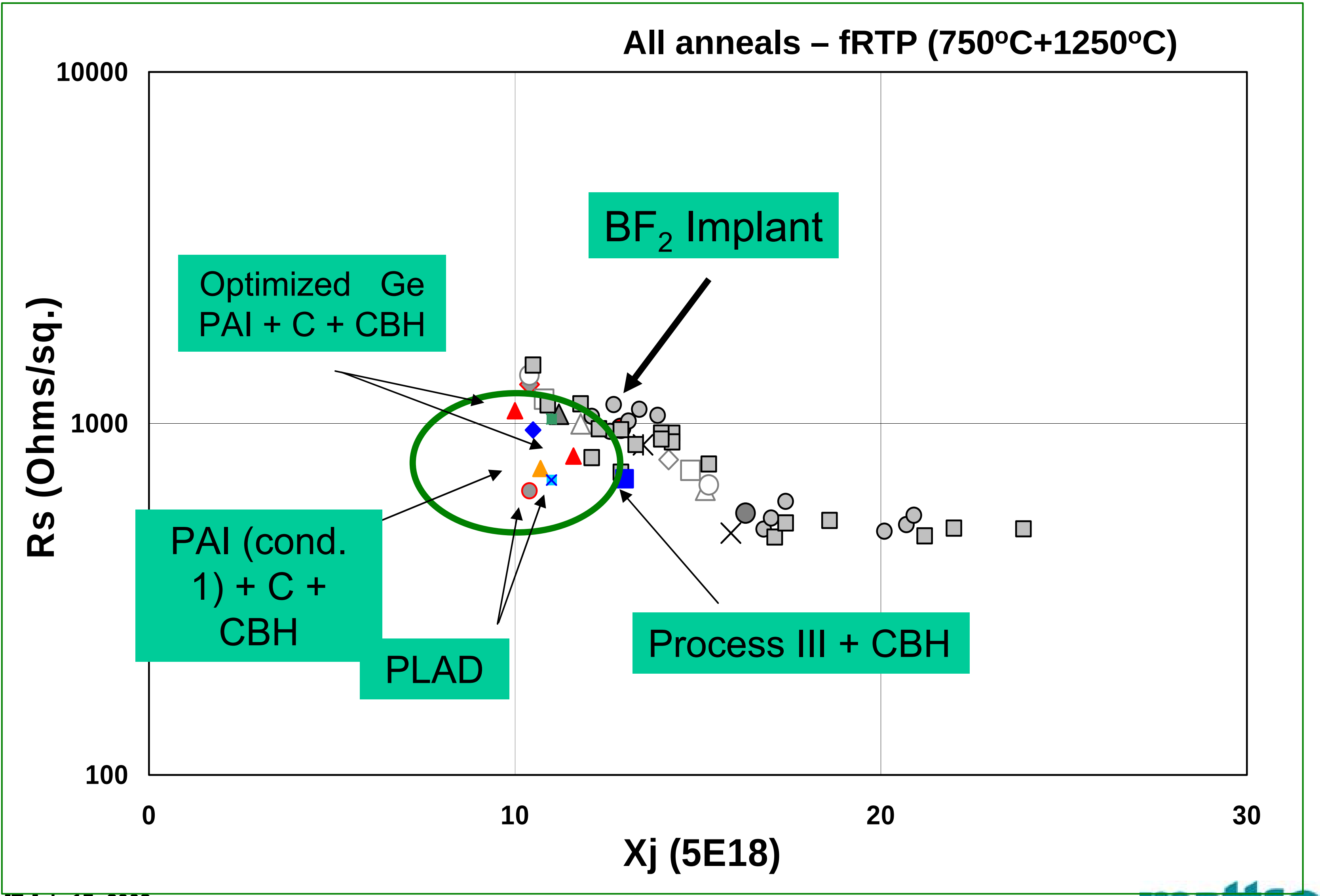
TEM showing no extended defects.

Summary of PLAD/fRTP Data



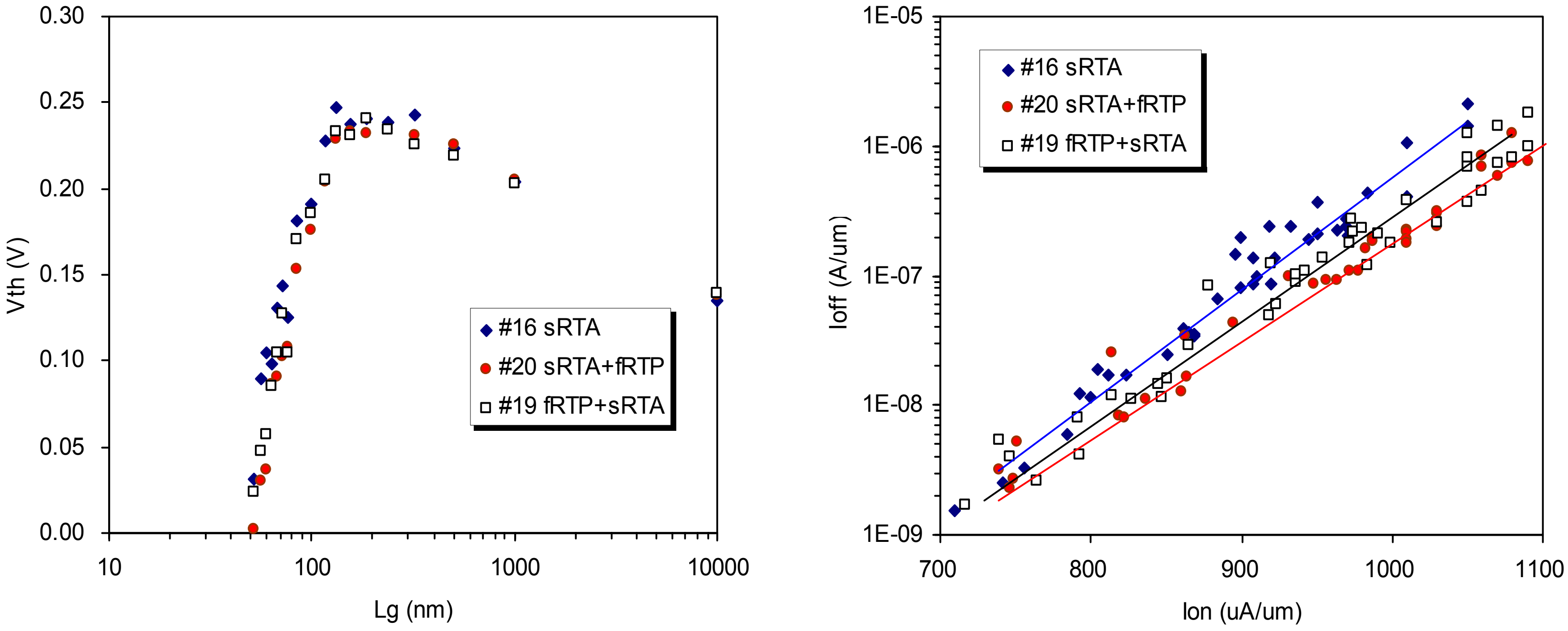
Summary of PCOR SIMS results of 250 eV B_2H_6 PLAD using various flash annealing recipes. The best performance is seen with the 750° C intermediate and 1250° C peak temperature.

Optimized Implant and Anneal Conditions Yield Superior Junction X_j/R_s



A Partner You Trust.
Performance You Value.

Transistor Performance Improvement



Threshold voltage vs. gate length showing no shift with spike + flash or flash + spike compared to standard spike anneal. The combination of spike and flash annealing gives a 4-6% improvement in NMOS drive current

LeIrch, et. al., IWJT-2007, Kyoto

Conclusions

- High quality, ultra shallow junctions can be achieved using advanced implant and annealing approaches:
  - Optimized PLAD implants/fRTP anneals produce junctions with R_s/X_j 11nm and 820 Ω/sq. demonstrated (@5E18cm^{-3})
  - Using beamline Carborane molecular implants, junctions with R_s/X_j 10.5nm and 960 Ω/sq. demonstrated (@5E18cm^{-3})

- Co-optimization of doping and activation is required to meet future junction performance targets