



Metrology of Defect Annealing in Advanced USJ Formation Processes

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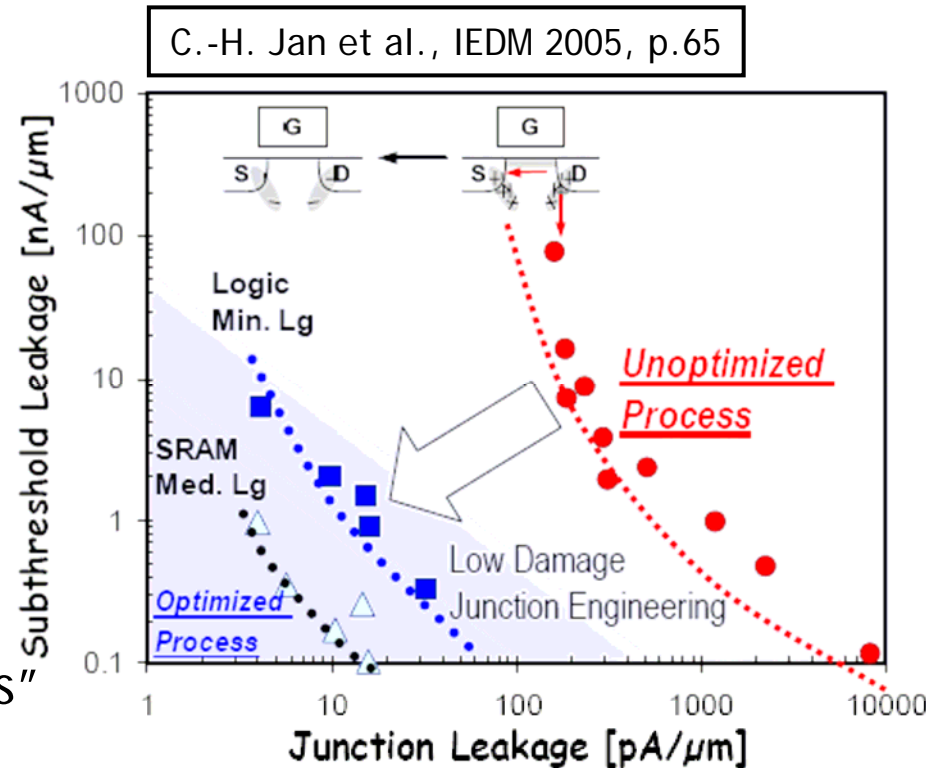
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Outline

- Introduction
 - Trade-offs in annealing
 - Metrology challenges
- Diffusion & Electrical Activation
- Damage annealing
 - Reflectance Spectra
 - Junction Leakage (RsL)
 - Photoluminescence
 - Thermal Wave
- Paths forward for advanced junction engineering
- Conclusions

Advanced USJ Requirements

- Minimize Dopant Diffusion
- Maximize electrical activation
- “Enough” defect annealing
 - Junction leakage: Becoming significant for low power CMOS
 - High channel/halo doping greatly increases leakage
- Need to optimize all 3 “dimensions”
- Damage metrology:
 - Traditional - TEM, devices
 - Non-Contact:
 - Reflectance
 - $R_sL - R_s$ & Junction Leakage
 - Photoluminescence
 - Thermal Wave



Rapid Process Optimization

Trends in Millisecond Annealing

- Currently, millisecond anneal is being combined with spike annealing
 - Polysilicon gate activation
 - Gate overlap
 - Implant damage recovery
- As technology progresses, the desire is to lower the thermal budget further
 - Reduce dopant diffusion
 - Metal gate / high-K integration
 - Strain engineering integration
- Reduce peak T of spike anneal or migrate to millisecond anneal only?
 - Residual defect concerns
 - Damage engineering - implant & anneal

Experiment

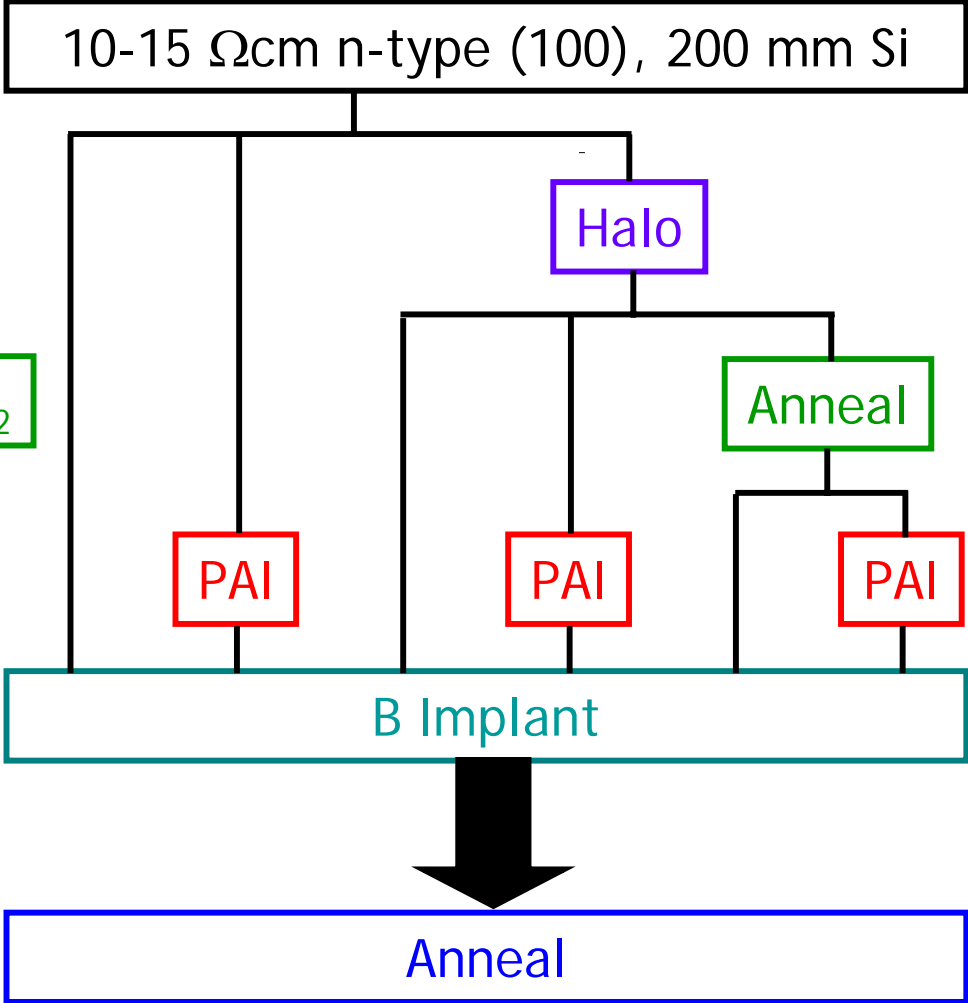
Halo: 4×10^{13} As/cm² @ 40 keV

Pre-anneal: 1050°C, 10 s, 10% O₂

PAI: 10^{15} Ge/cm² @ 30 keV

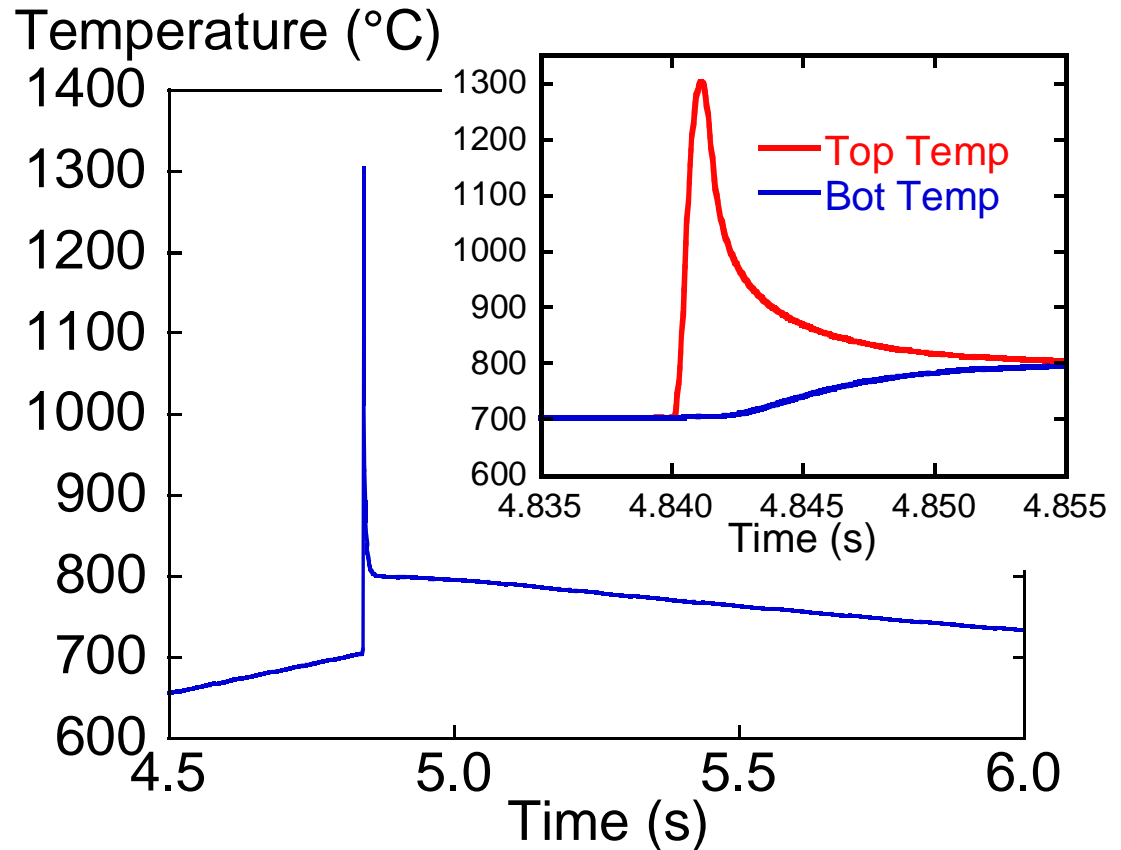
B: 10^{15} B/cm² @ 500 eV

Anneals:
• SPE: 650°C, 5 s
• Spike: 1050°C
• fRTP: Various conditions



Millisecond Annealing with Flash-Assisted RTP™

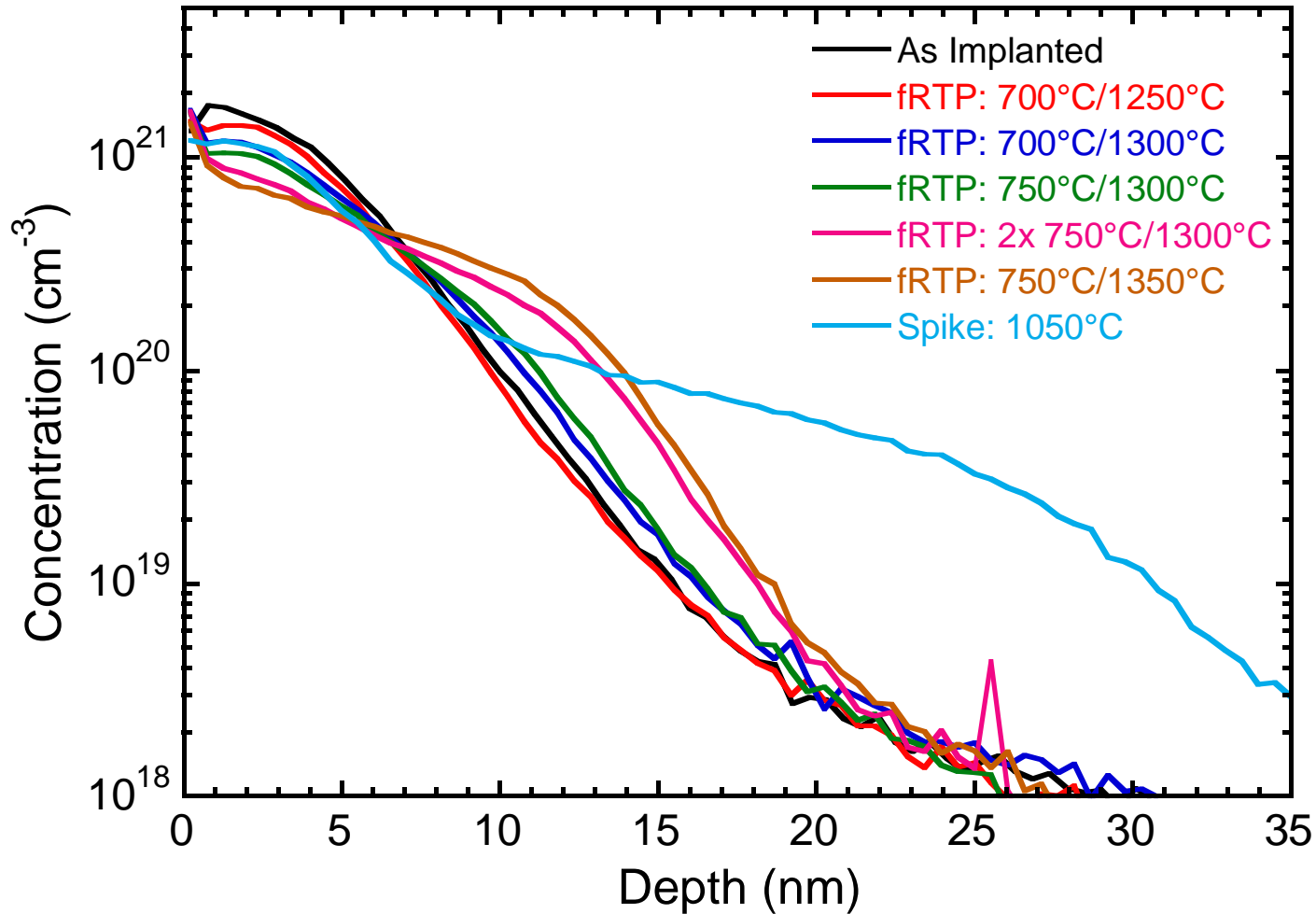
- Flash-Assisted RTP™ (fRTP™):
 - 150 K/s ramp to T_i
 - Pulsed surface heating
 - Millios™ tool provides real-time T measurement on front & back of wafer



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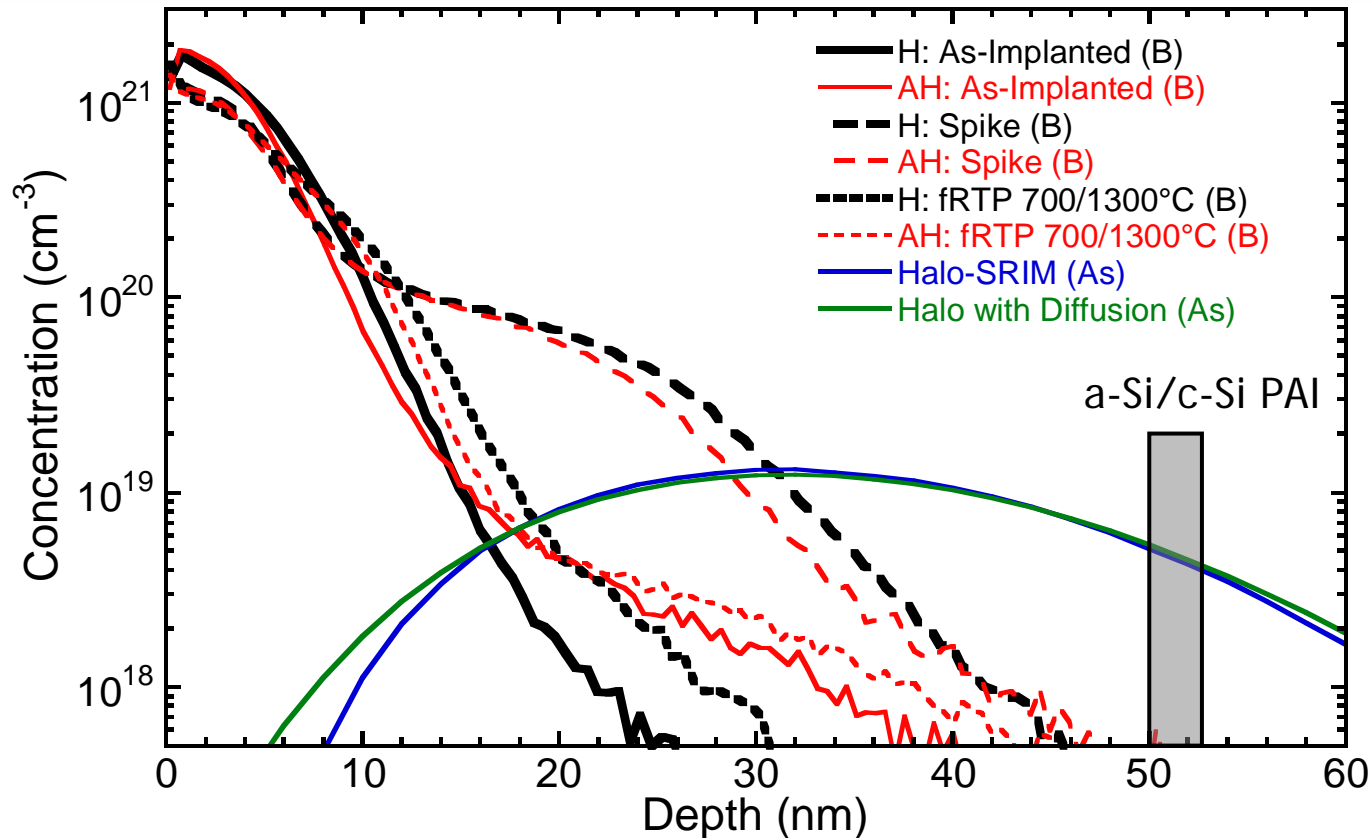
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Diffusion Behaviour in c-Si Wafers



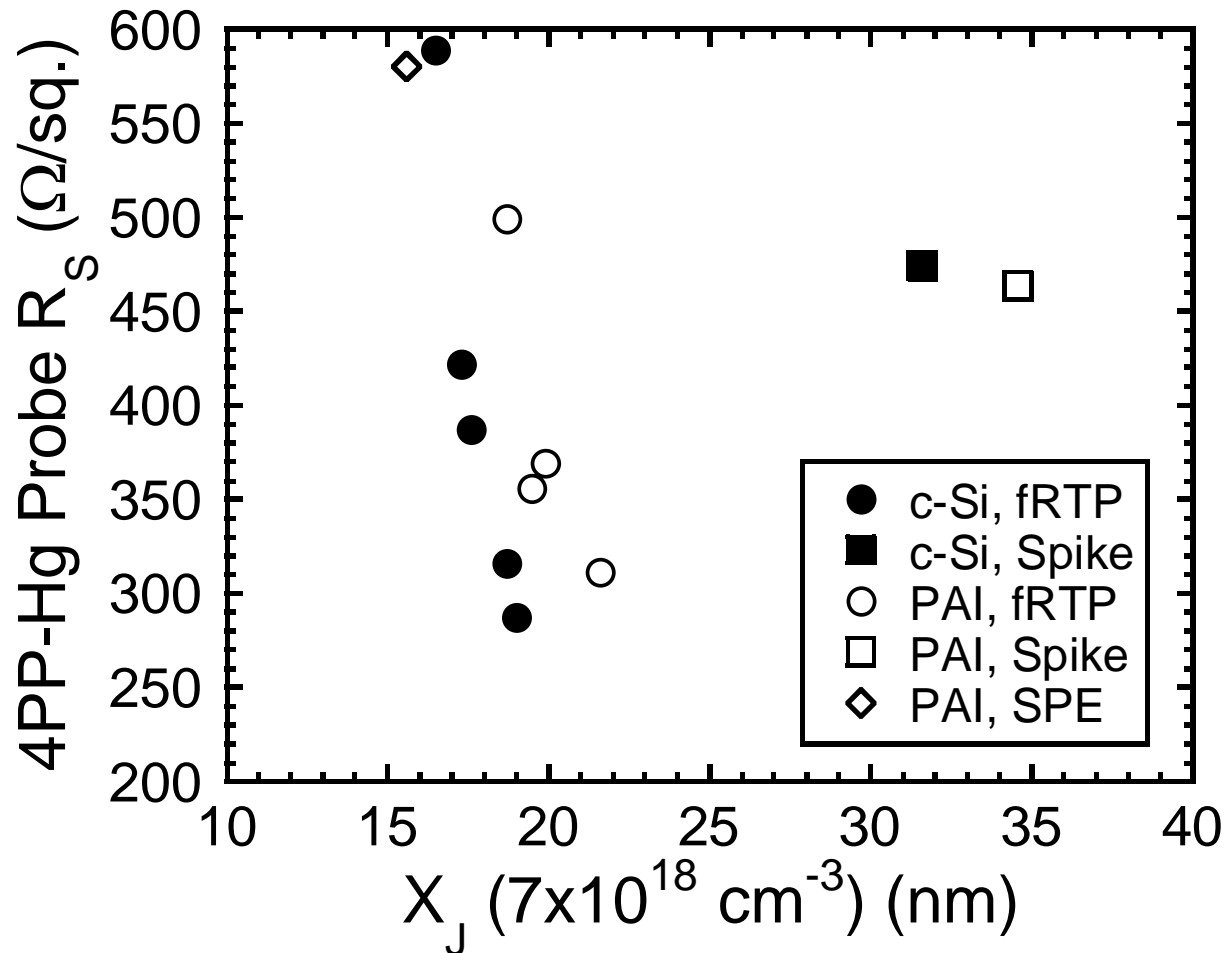
- Minimal diffusion with fRTP, except for highest t_{eff}
- Concentration-enhanced diffusion \Rightarrow More abrupt junctions

Halo Doping and Pre-Annealing Effects (c-Si Case)



- Halo suppresses B ion channelling, but introduces TED
- Pre-annealing halo \Rightarrow Behaviour similar to c-Si case
- Expect high junction leakage with halo
 - Junctions at $\sim 15\text{-}30$ nm depth, doping $> 6 \times 10^{18}/\text{cm}^3$
 - High doping concentration: \Rightarrow Narrow depletion region (~ 15 nm)
 - Residual damage from PAI and halo implants

fRTP: Improved Activation & Reduced Diffusion

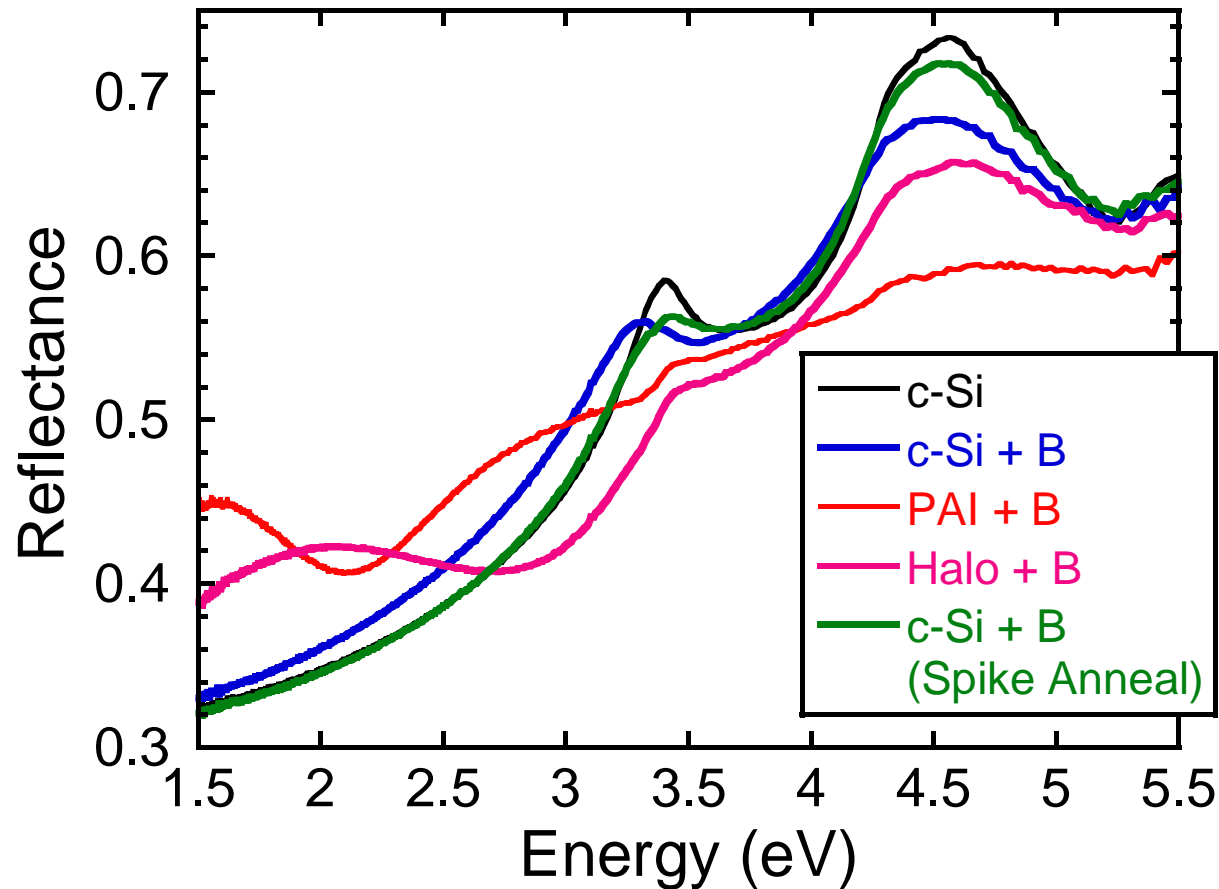


- fRTP gives a major improvement over spike anneal in R_s/X_j trade-off for both c-Si & PAI
- No benefit evident for use of PAI over c-Si

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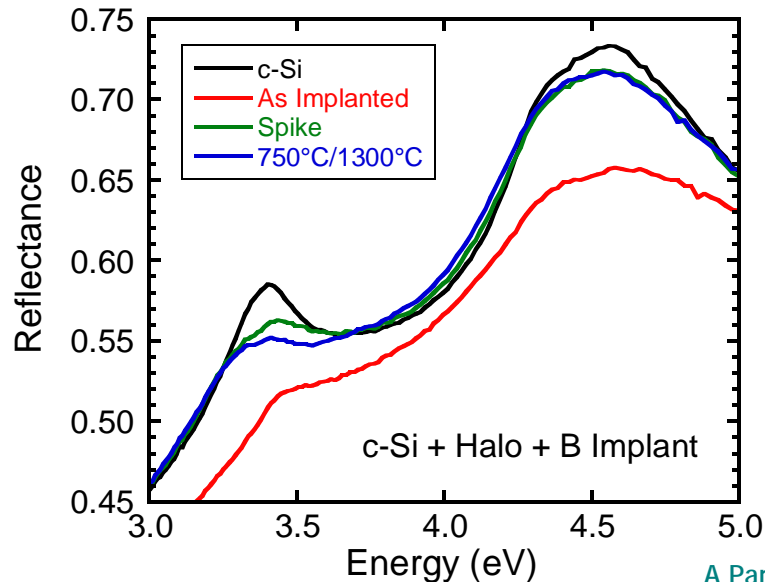
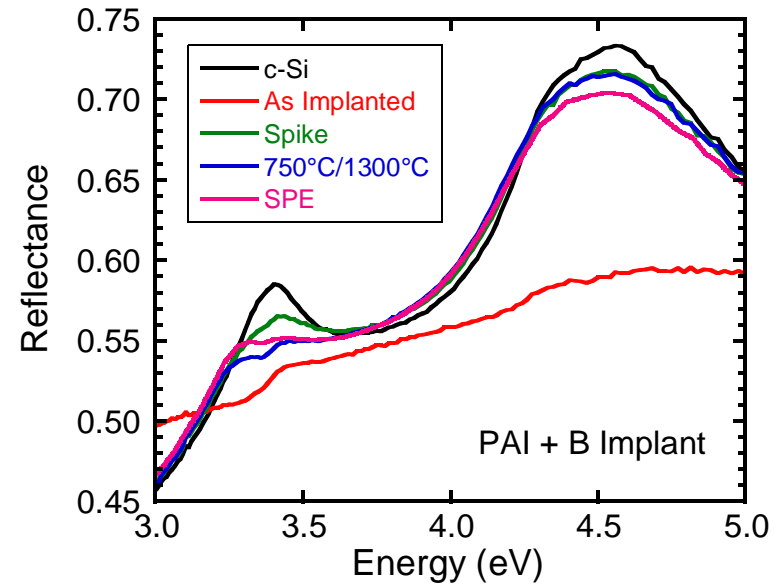
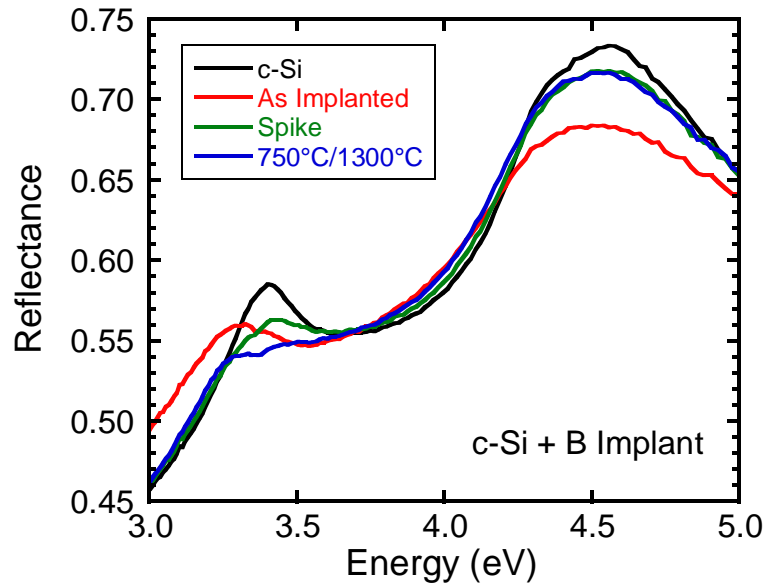
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Reflection Spectra Reveal Implant Damage



- Peaks at 3.4 and 4.6 eV reflect “long range” crystalline order
 - Disrupted by implant damage
- Oscillations < 3 eV \Rightarrow amorphous layer
 - ~ 50 nm thick for PAI; ~ 30 nm for halo (heavy damage layer)

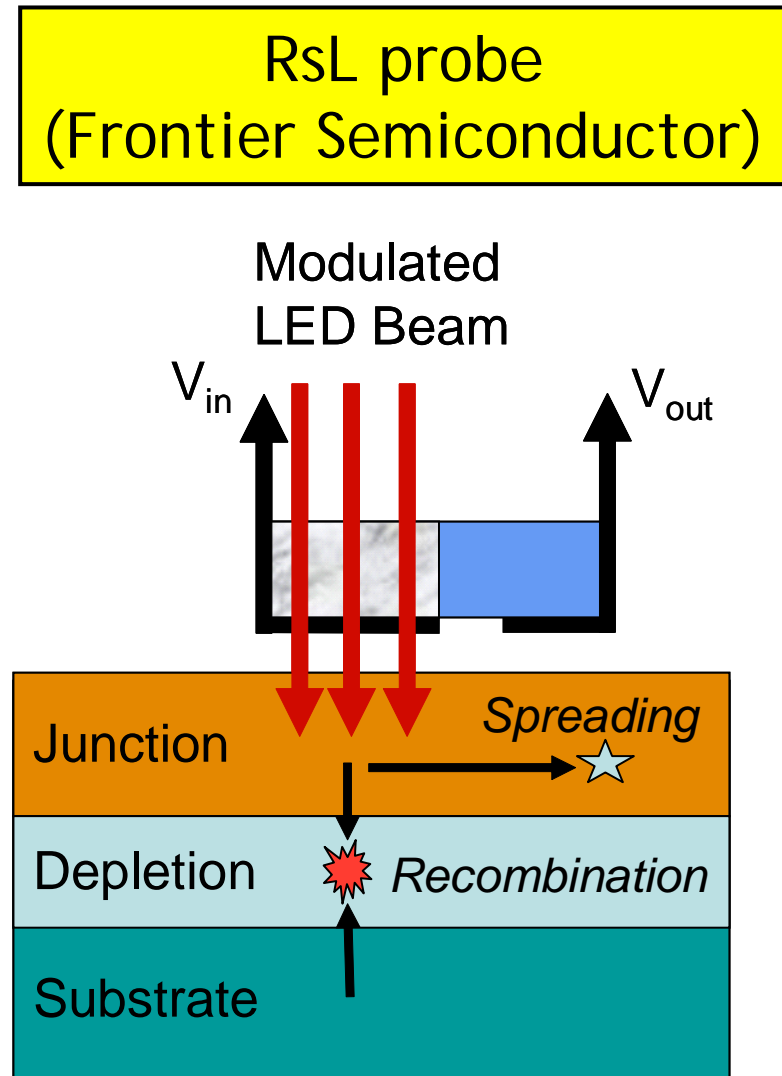
Evolution of Reflectance Peaks with Annealing



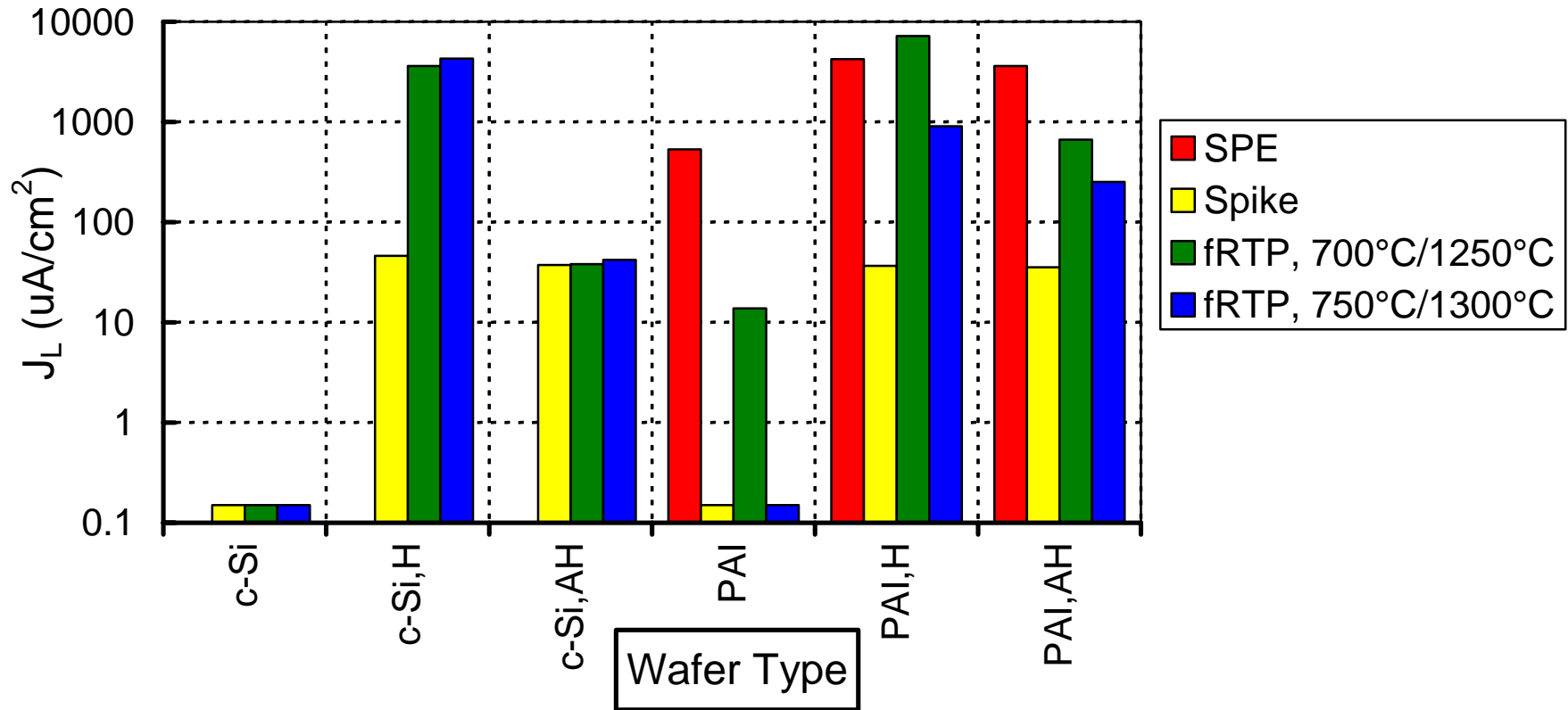
- Behaviour at peaks is sensitive to annealing, especially 3.4 eV peak
- At 3.4 eV light penetrates ~10 nm
⇒ Probes heavily B-doped region
- More sophisticated analysis should be possible

RsL™: Non-Contact Sheet Resistance & Leakage

1. Modulated light source creates free carriers in junction & substrate.
2. Carrier drift & leakage monitored by dual-probe measurement of junction photovoltage (JPV).
3. Carrier spreading analysis gives sheet resistance, R_S .
4. Frequency dependence of JPV gives recombination leakage current, J_L .

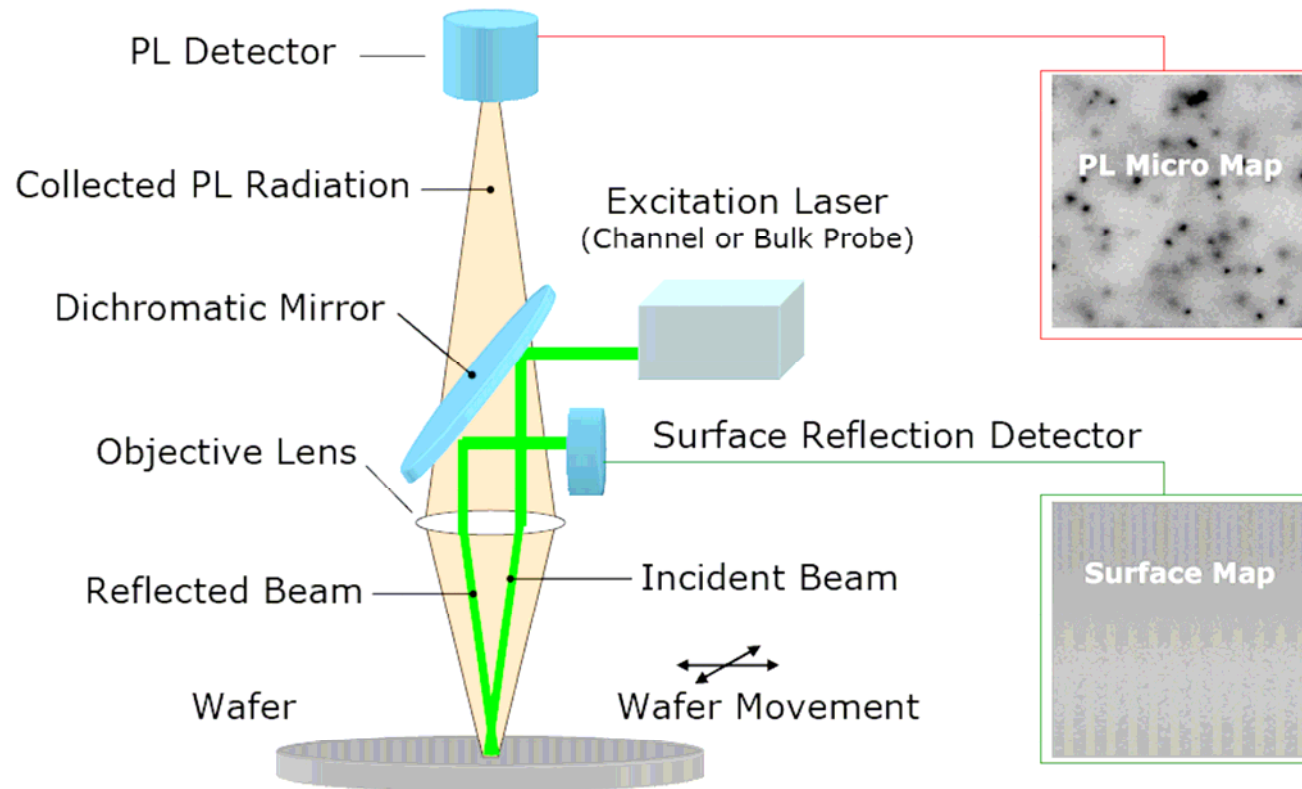


Junction Leakage Reveals Dominant Role of Halo



- Halo doping greatly increases leakage (narrow depletion region)
 - Pre-annealing halo damage reduces J_L , esp. in c-Si
- For PAI, 1300°C fRTP significantly reduces J_L from SPE level

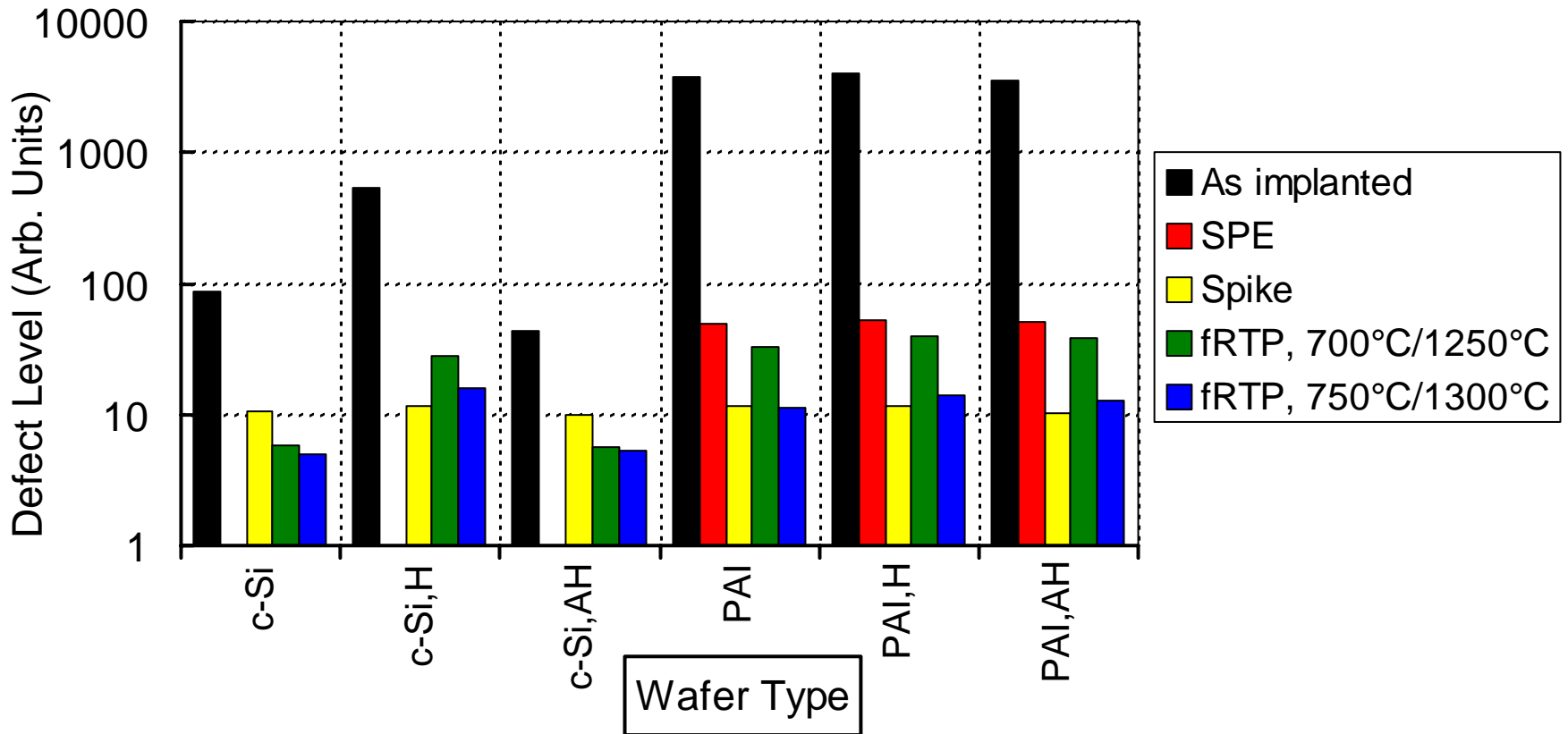
Photoluminescence for Damage Characterization



A. Buczkowski,
ECS Trans. 11(3)
p.109 (2007)

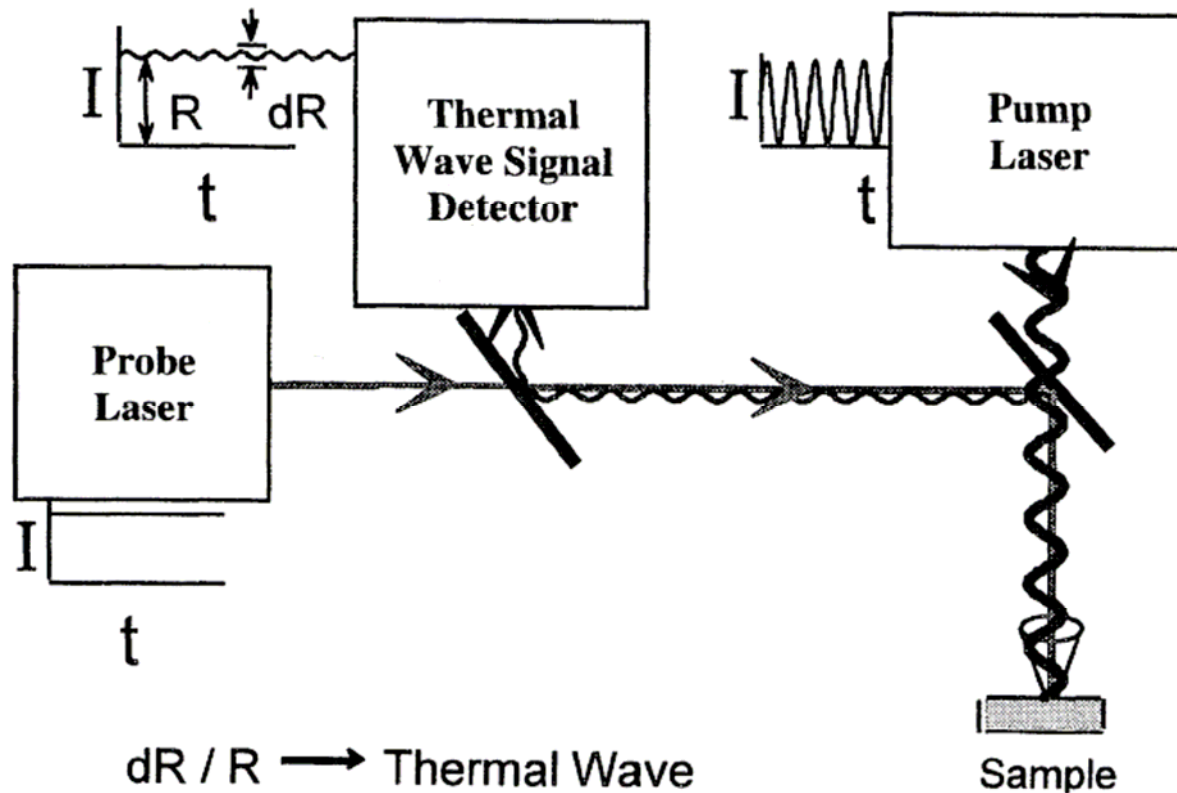
- Room temperature photoluminescence measurements were performed using a system from Accent (Now Nanometrics)
- The PL signal is very sensitive to defects that alter electron-hole recombination behaviour

Photolumuminescence Shows Damage Annealing Trends



- For c-Si, halo damage effect and annealing trend are evident
- With PAI, halo condition makes little difference
- 1300°C fRTP \Rightarrow Damage levels \cong spike annealing result

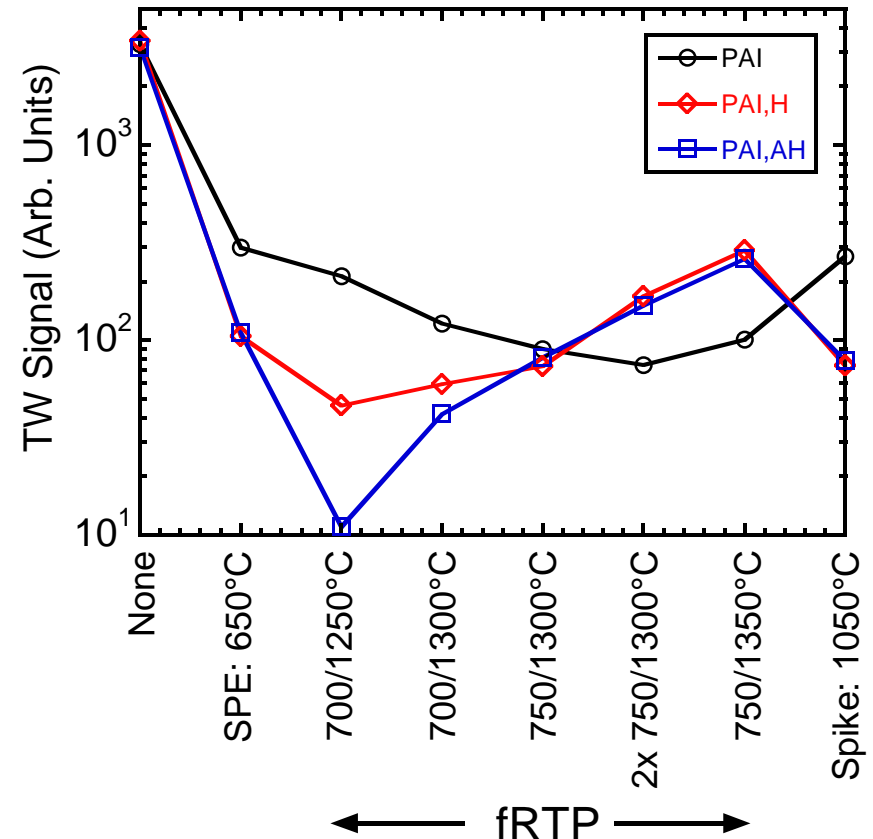
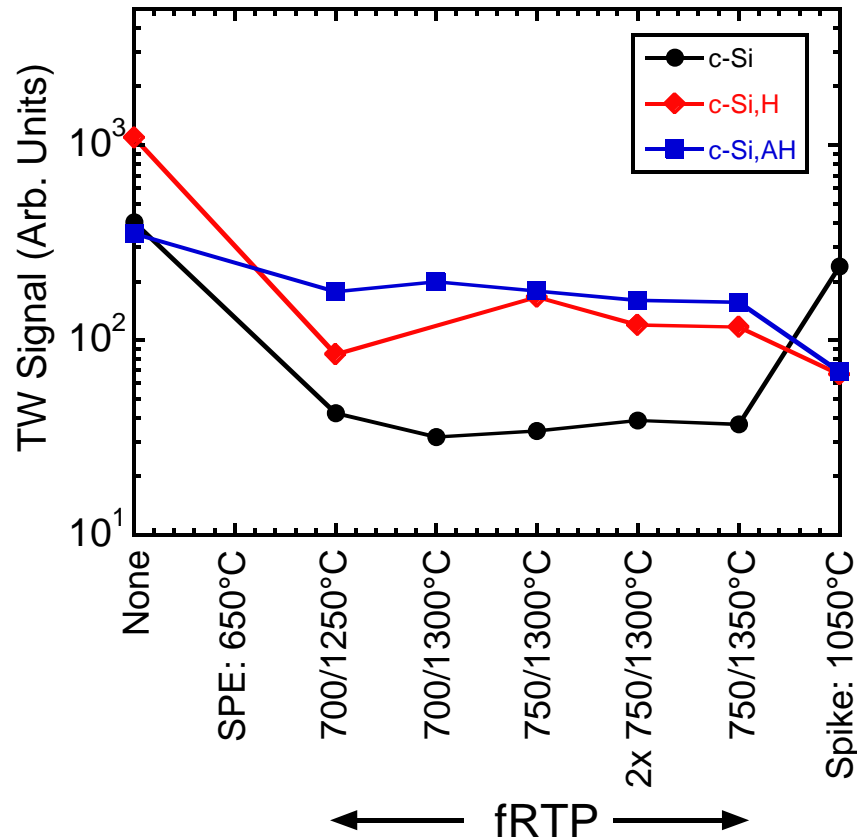
Thermal Wave Characterization



S. Cherekdjian et al., ECS PV 2002-11, (2002) p.339

- Thermal wave measurements were performed using a TP630XP system from KLA-Tencor
- The TW signal can be affected by both defects and by doping distributions

Thermal Wave Results Reveal Doping & Damage Phenomena



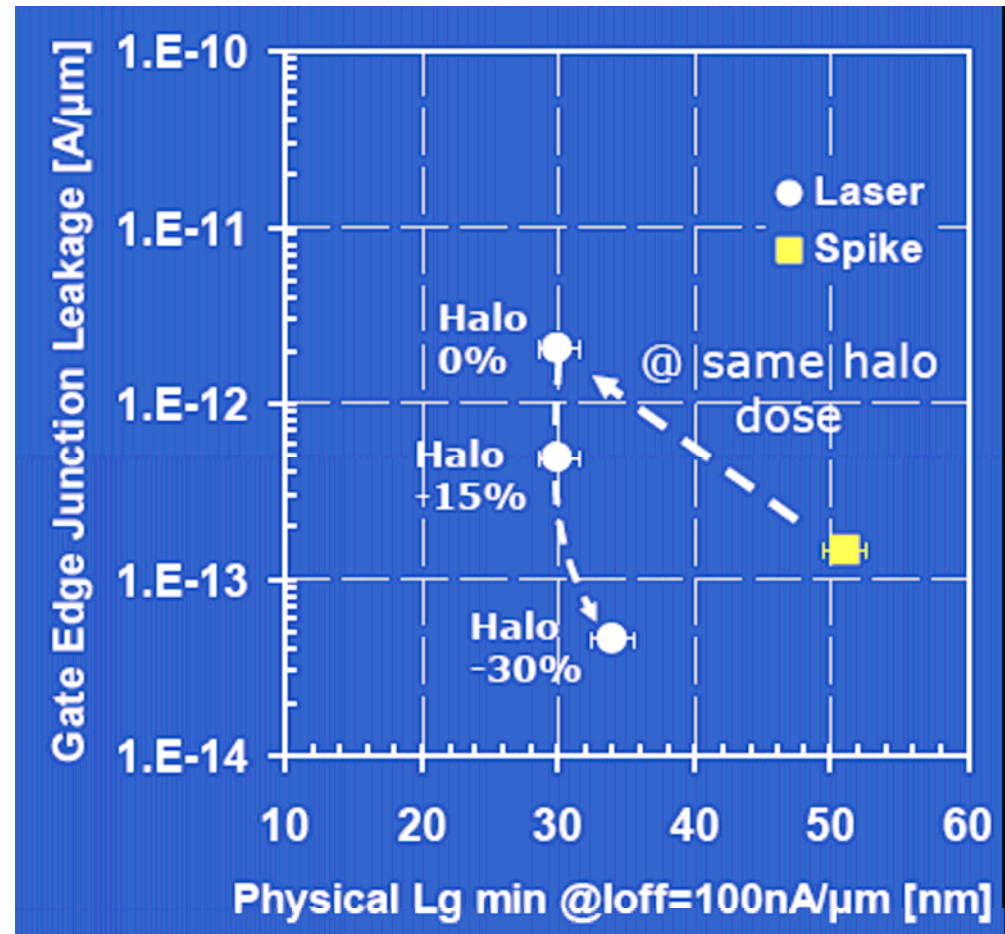
- TW Signals initially reduce with annealing
- Halo implant has large effect on final signal values
 - But, pre-annealing has relatively little effect
- Results suggest that doping plays a key part in the TW signal

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Minimizing Halo Doping is Essential for Leakage Control

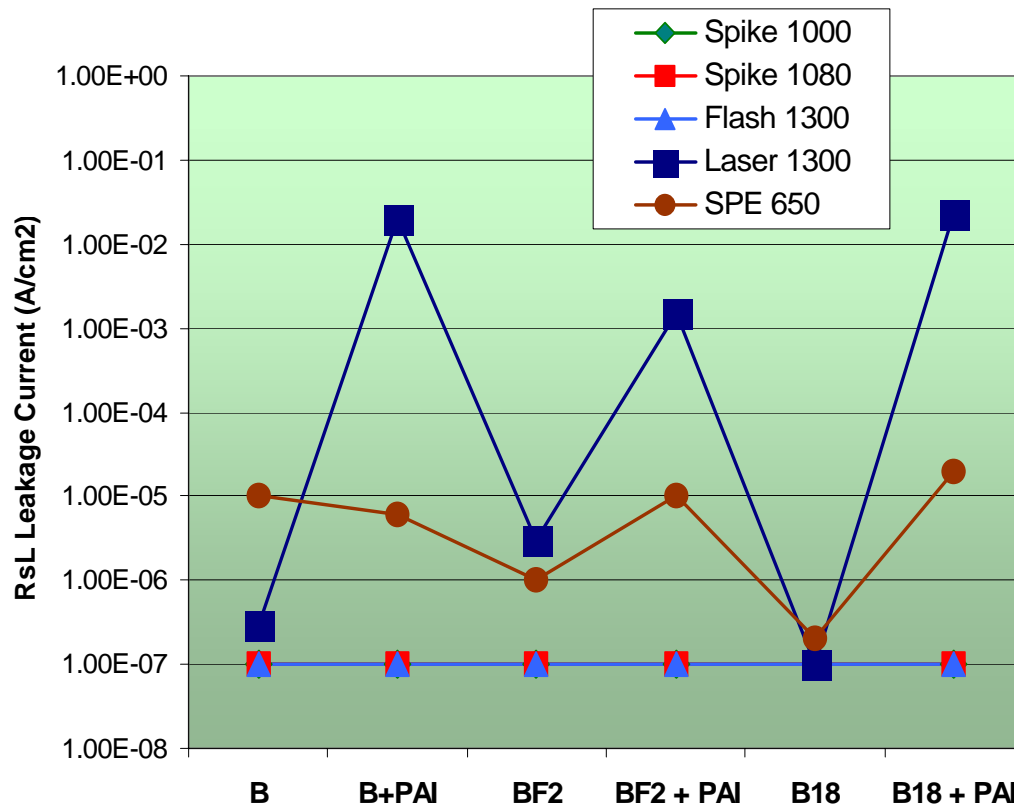
- Millisecond Annealing enables shallower junctions and hence improved short-channel effect control
 - Halo dose can be reduced
 - Reduced BTBT
 - Reduced damage from halo



T. Hoffmann et al., IIT 2008 Conference, Monterey, 2008

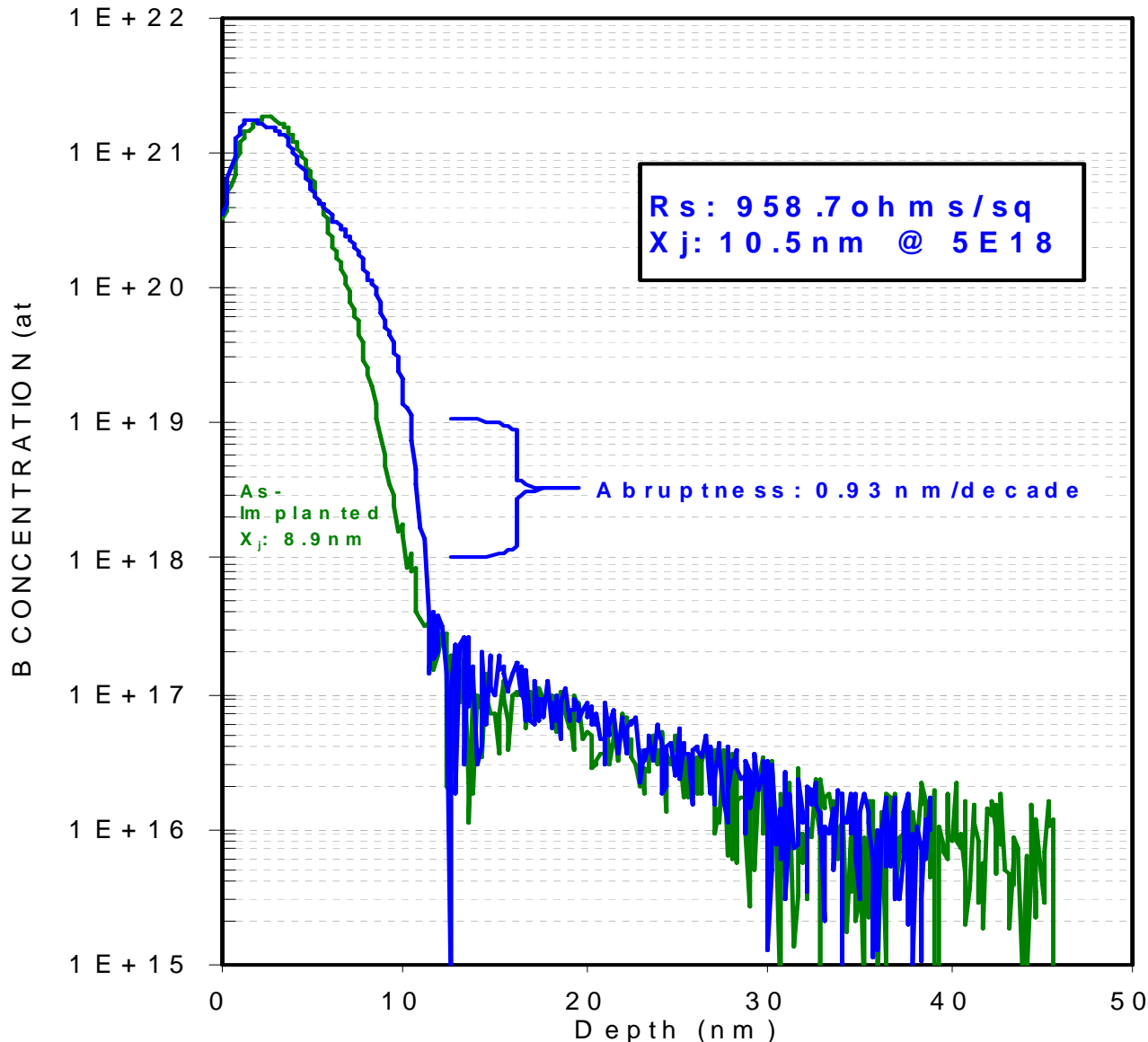
Damage/Activation/Diffusion Engineering Requires Innovation in BOTH Implantation and Annealing

- Selection of implant approach has major effect on residual damage:
 - PAI & dopants: Mass, dose, energy, dose rate, temperature
 - Co-implants: Diffusion & activation control
 - Novel implant schemes: Molecular implants, plasma doping, GCIB



$B_{18}H_{22}$ implant shows greatly reduced RsL leakage current (SemEquip data)

Boron Doping Profile: Carborane Implant and MSA



SIMS profile of flash annealed carborane implant. Note superior X_j/R_s and junction abruptness

*J. Gelpy et al.,
Ultra-Shallow
Junction Formation
using Flash Annealing
and Advanced Doping
Techniques, IWJT-
2008.*

Conclusions

- The halo implant is dominant in determining junction leakage:
 - Dose and halo implant damage are critical
 - Pre-annealing halo damage reduced leakage
- Annealing approaches offer trade-offs :
 - Spike anneals remove defects, but introduce excessive diffusion
 - SPE gave good activation with very little diffusion, but junctions show severe leakage
 - Millisecond annealing with fRTP showed improved activation with minimal diffusion, as well as improved defect annealing
- Novel metrology techniques \Rightarrow very rapid assessment of defect phenomena & optimization of implant & annealing choices
- The next steps in USJ technology require advances in both implantation and annealing
 - Novel implantation methods can help overcome the damage annealing challenge

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