Strain Effects In Millisecond Laser Annealing

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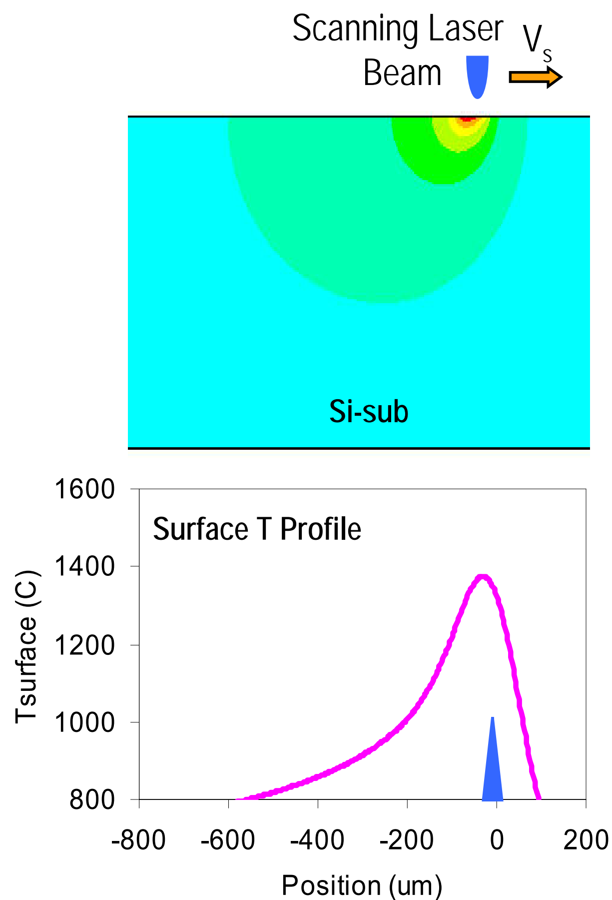
Outline

- Laser annealing temperature and thermal stress profiles
- Warpage & stress characterization using CGS technology
- e-SiGe challenges & warpage reduction
- Laser annealing for e-SiC
- Summary

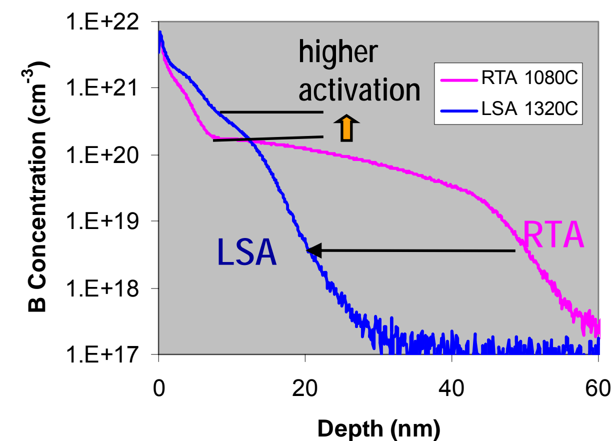
Millisecond Laser Annealing



Temperature (°C)
400 600 800 1000 1200 1400
Depth (um)
0 200 400 600 800
Depth T Profile

(a) Laser annealing T profiles

- Laser heating is localized both laterally & vertically
- Annealing time can be controlled by scan speed
- high T, short duration results in shallower junction with higher activation

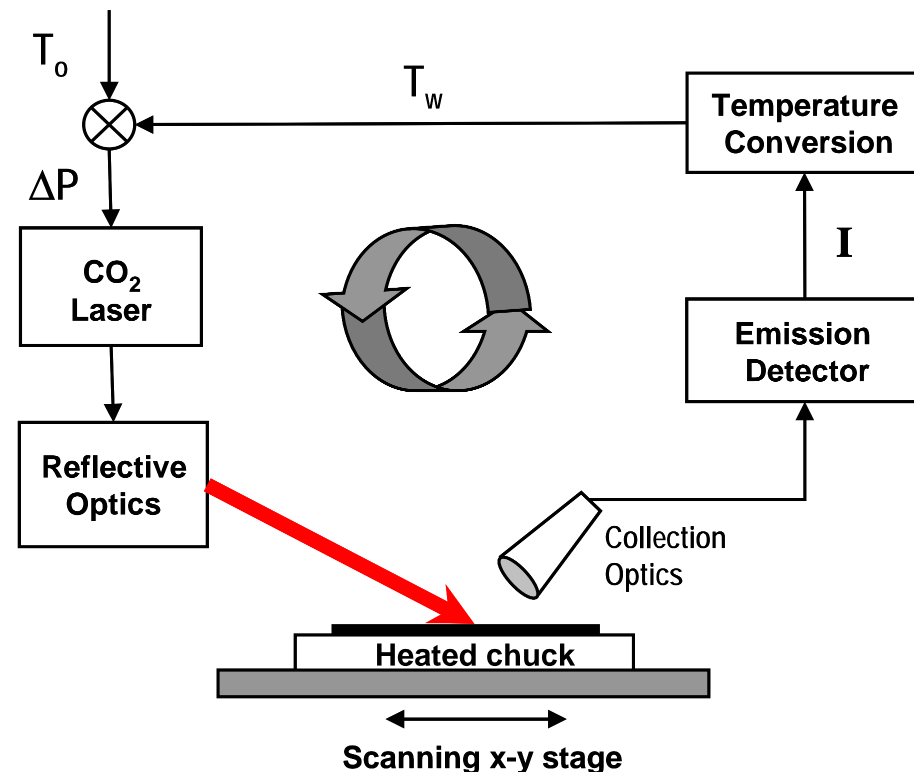


(b) Junction profiles: LSA vs RTA

Ultratech's Laser Spike Annealing System

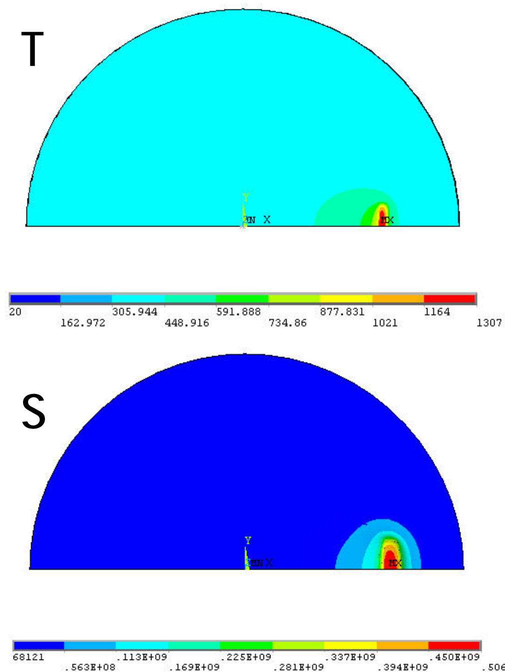
Key Attributes

- CO2 Laser
- P-polarized
- Brewster angle incidence
- Temperature feedback control

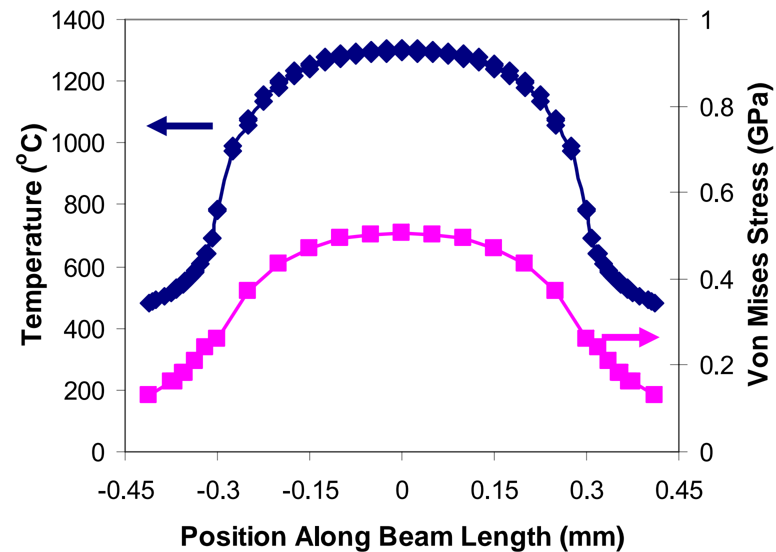


3D Thermal Stress Simulation Results

(a) Thermal & stress contours



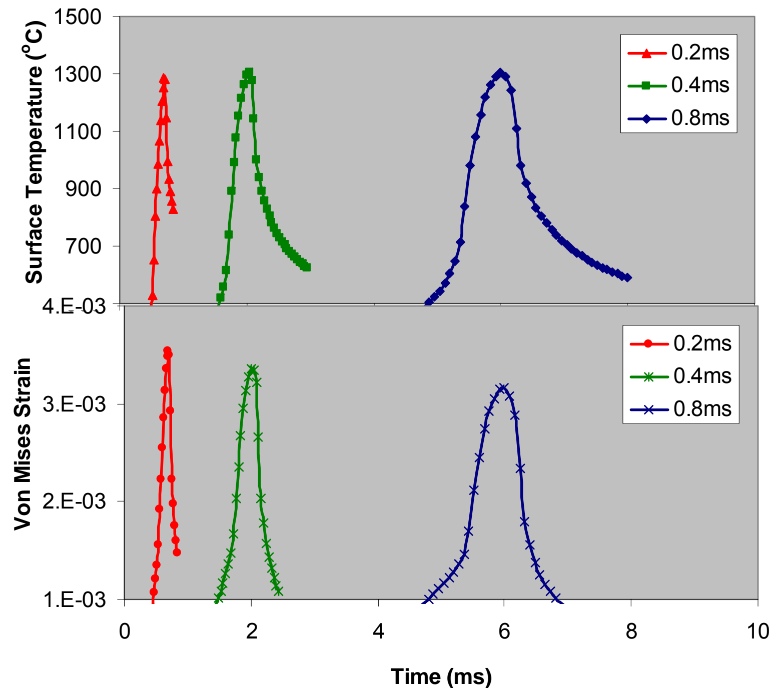
(b) Surface cutline along beam length



- **Von Mises stress profile roughly follows temperature distribution.**

Thermal Stress vs. Dwell Time

Simulate temperature & stress



Max Von Mises stress vs dwell

T_{pk}~1300°C

t_d (ms)	Max S_{VM} (GPa)
0.2	0.580
0.4	0.538
0.8	0.506

- **Max thermal stress increases with reduced dwell time.**
- **But dependence is weak, 15% change from 0.8ms to 0.2ms.**

Yield Stress Depends On Strain Rate

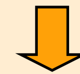
Haasen's Model:

$$\sigma_E(T,\dot{\epsilon}) = H(\dot{\epsilon})^{1/n} \exp[U/nkT]$$

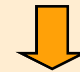
σ_E = yield stress
$\dot{\epsilon}$ = strain rate (sec^{-1})
U = activation energy
n and H are constants

n~2.1 is Silicon

Short dwell time



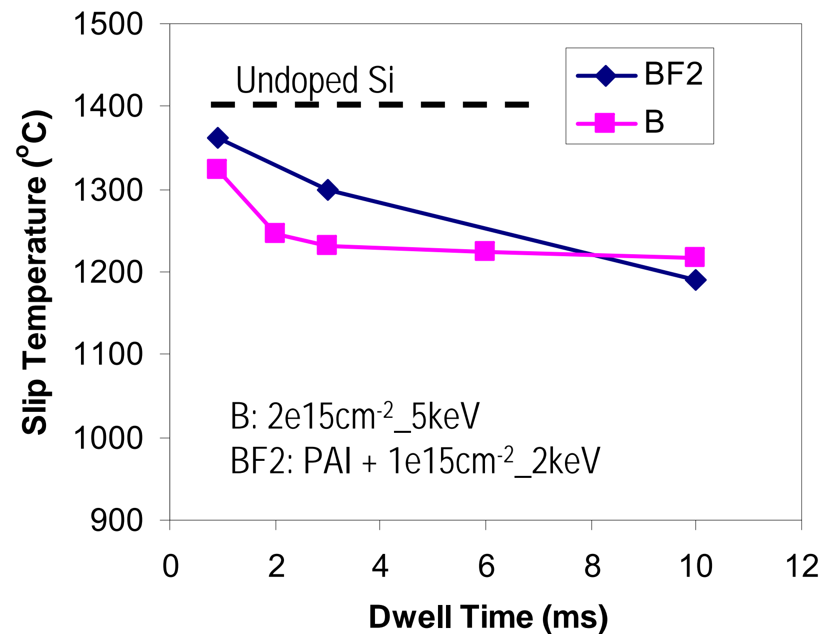
High strain rate



Increased yield stress

- **Yield stress can be increased by high strain rate at short dwell time.**

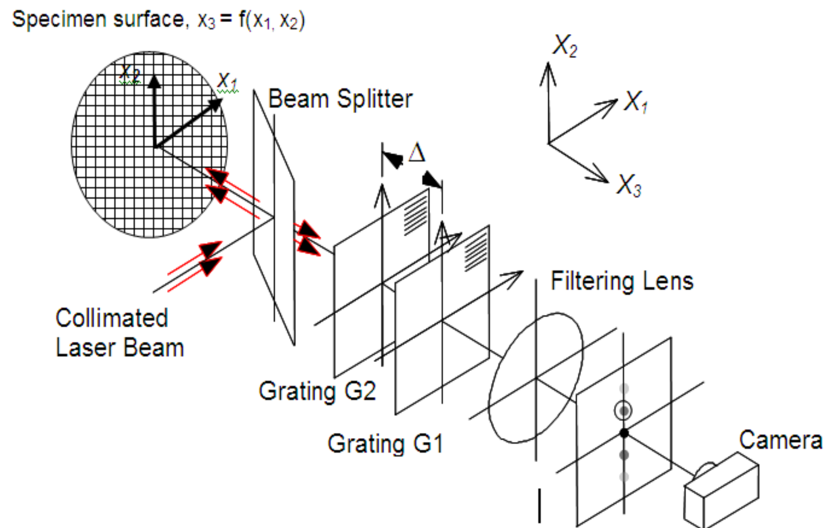
Slip Threshold vs Dwell Time

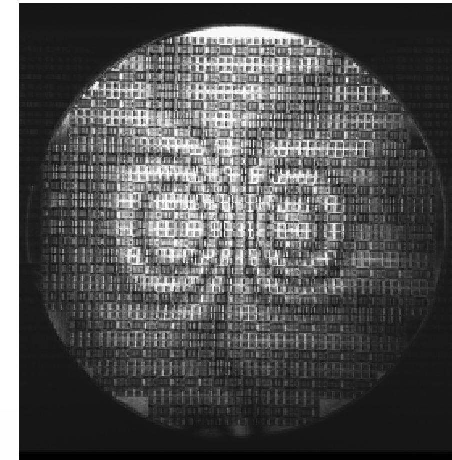


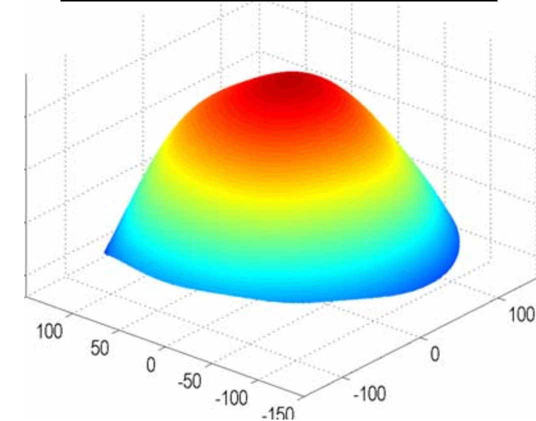
Longer dwell time lead to lower slip temperature

CGS Technology For Warpage & Stress Characterization

Warpage Measurement By CGS Technique



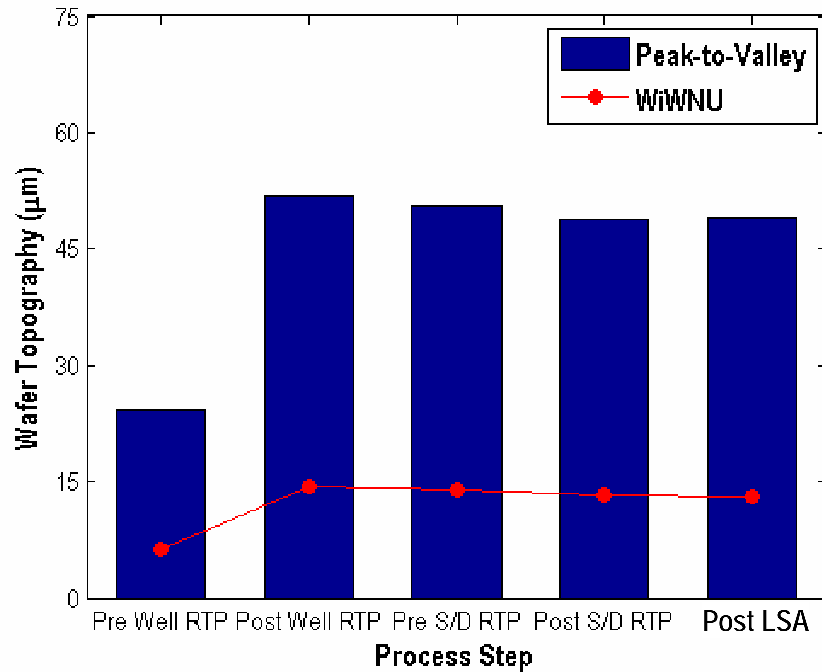




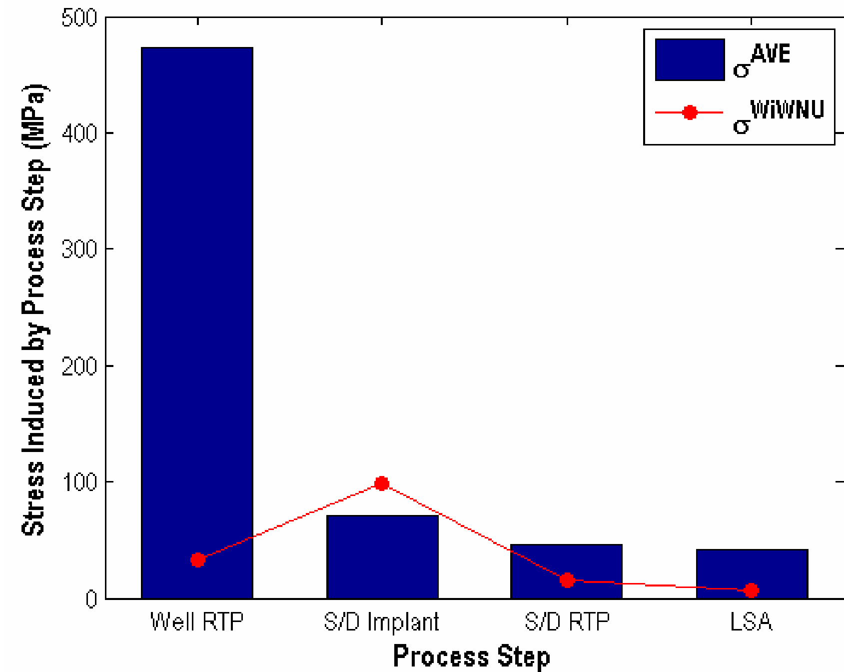
Full wafer topography & stress

- Coherent Gradient Sensing technology
  - Lateral shearing interferometer
  - Full Wafer: >600,000 points (310 μm per pixel)

Stress Fingerprinting

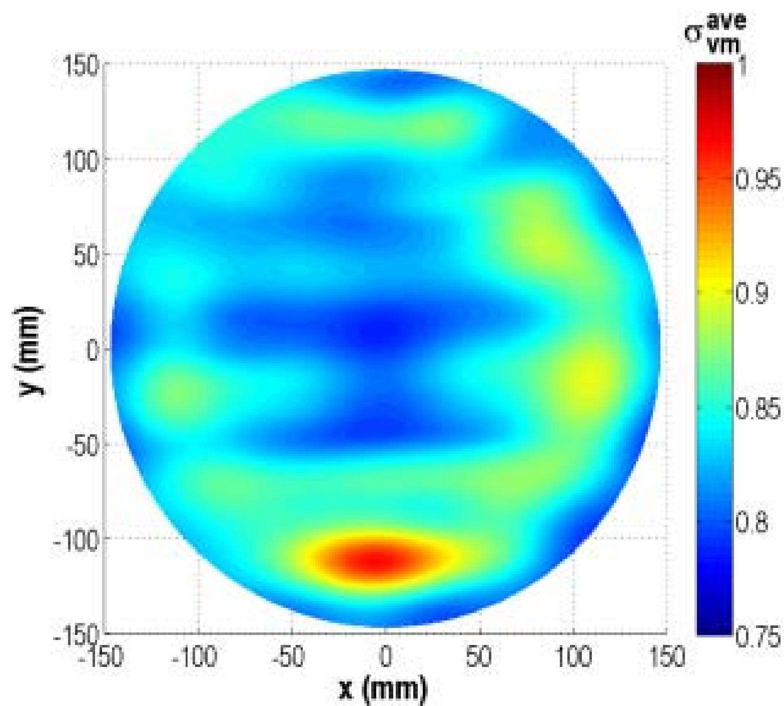


Topography Fingerprinting

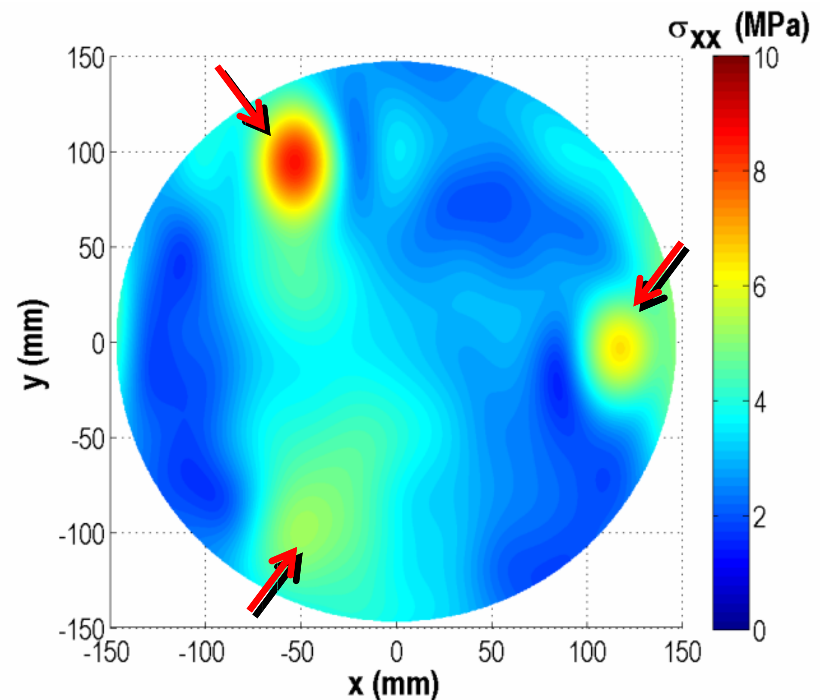


Stress Fingerprinting

Tool Features Shown By Stress Mapping



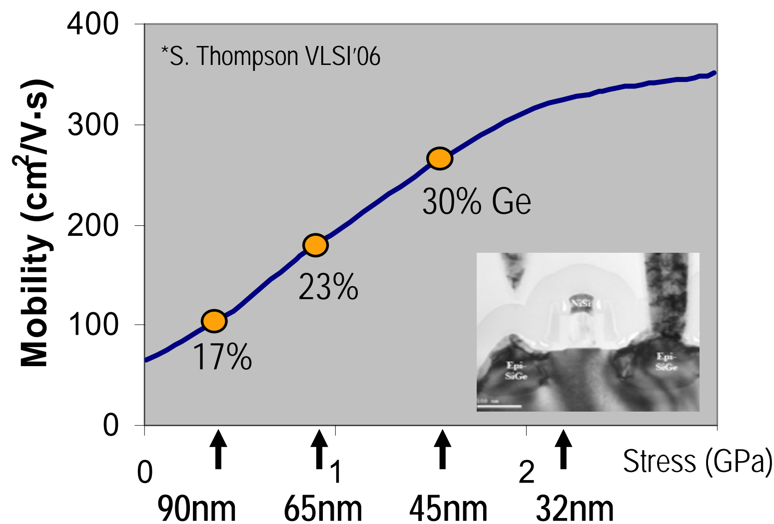
(a) RTP induced non-uniformity (average of 24 wafers)

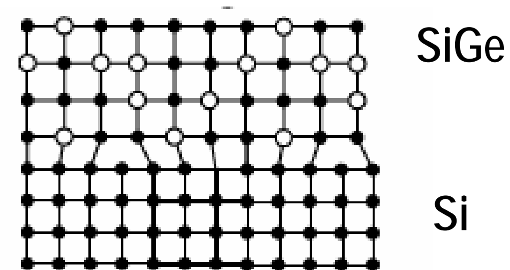


(b) Pin-signature from a different process

SiGe Wafer Warpage Reduction

Challenges With e-SiGe Devices





e-SiGe Issues:

1) Lower melting T
2) Dislocation generation & wafer warpage

Dislocation nucleation:

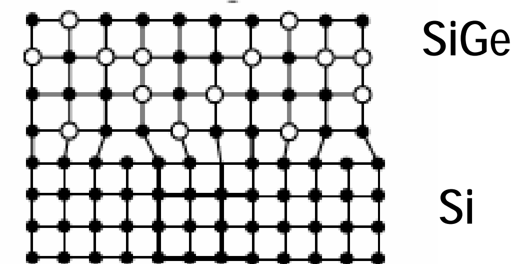
$$\frac{dN(t)}{dt} \propto N_0 \tau_{eff}^n \exp\left(-\frac{E_a}{kT}\right)$$

Dislocation propagation:

$$V \propto V_0 \tau_{eff}^m \exp\left(-\frac{E_b}{kT}\right)$$

(*Source: Houghton, et al, JAP 1991)

Effective Stress In SiGe



Source: Houghton, et al, JAP 1991

$$\tau_{eff}\,(\mathrm{GPa}) = 3.88\left(x - \frac{0.55}{h}\ln 10h + 24\Delta\alpha\Delta T \right) + \tau_{ms}$$

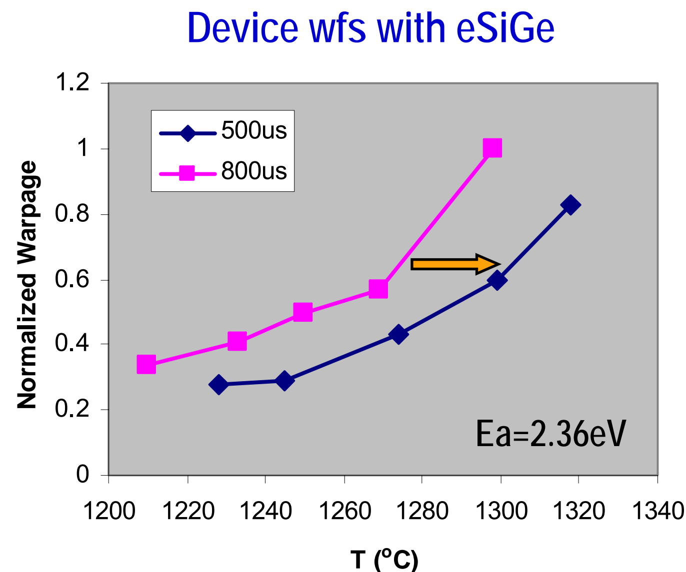
misfit stress

stress relief by single misfit dislocation formation

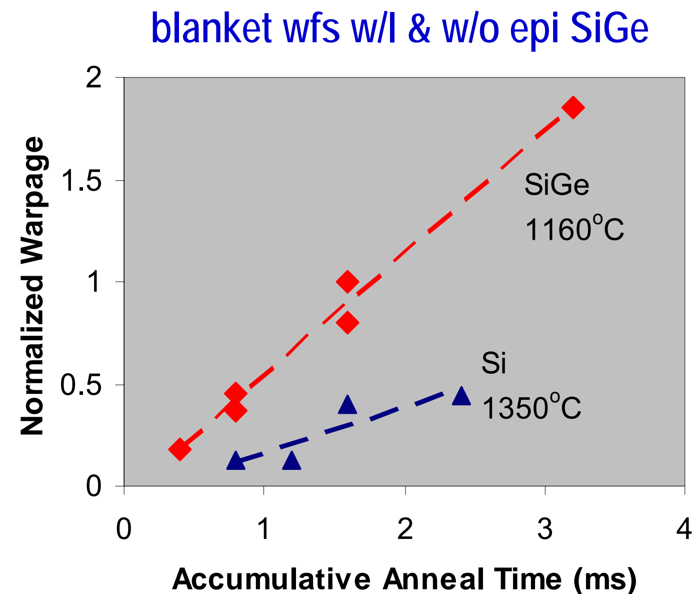
stress induced by differential thermal expansion between Si and SiGe

stress induced by thermal gradient due to surface heating

Warpage Reduction By Short Dwell Time



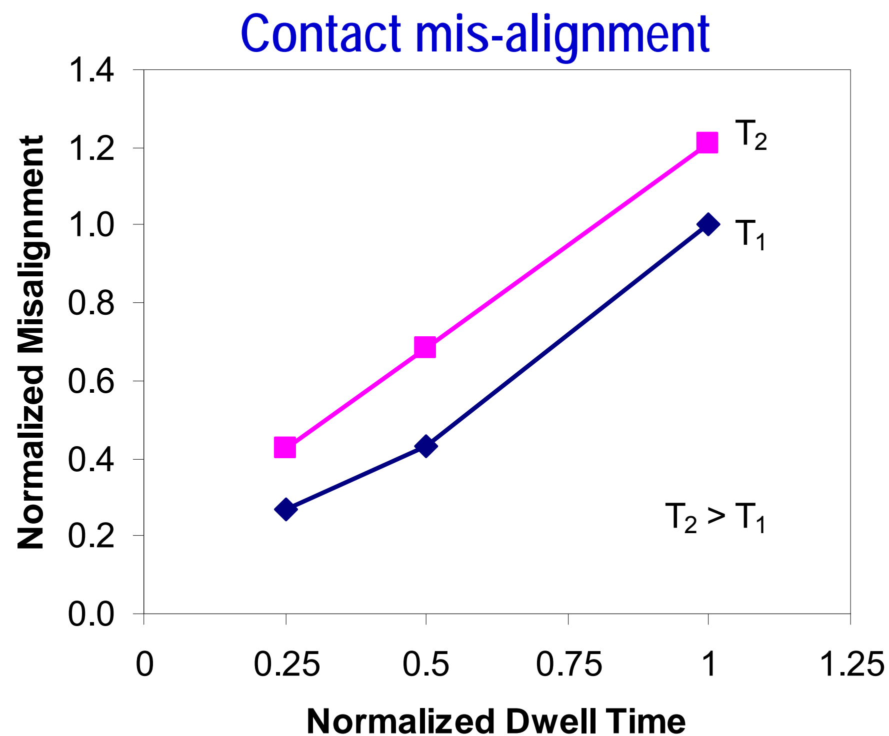
(a) Warpage vs T for 2 different dwell



(b) Warpage vs accumulative dwell time

- **Short dwell time enables higher annealing temperature or reduces warpage for the same annealing temperature.**

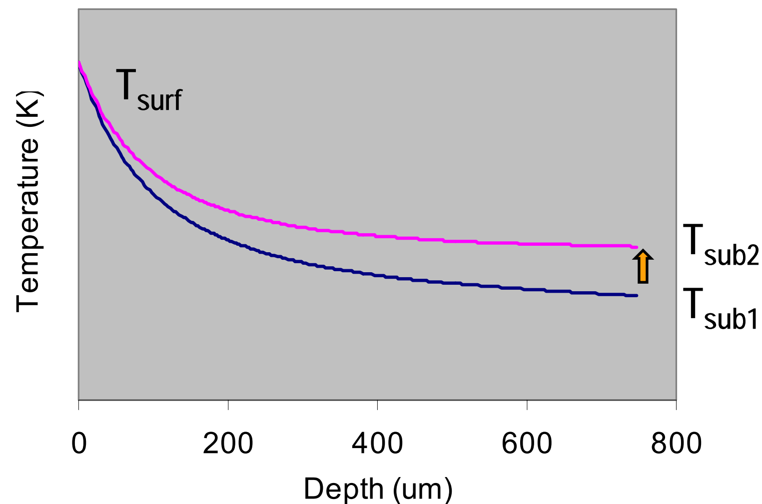
Impact On Litho Mis-Alignment



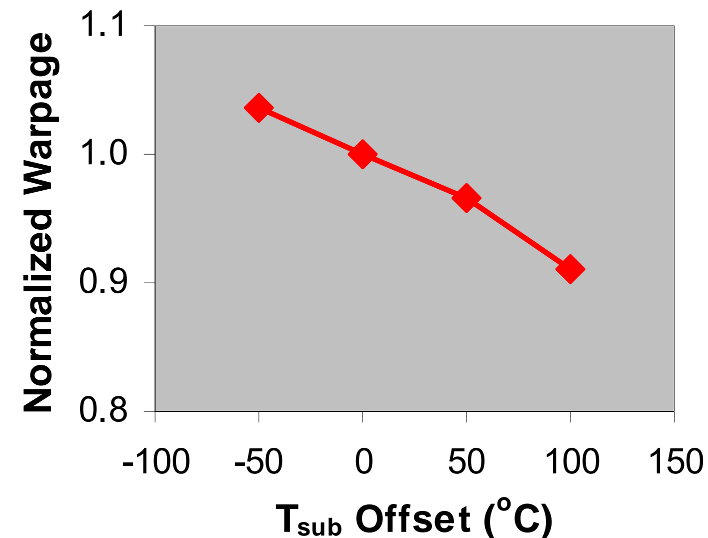
- **Short dwell time or lower annealing temperature reduces litho mis-alignment error.**

Effects of Substrate Heating

(a) Vertical temperature profile



(b) Warpage vs Tsub

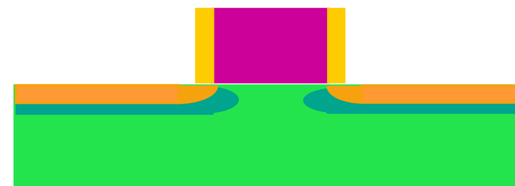


- Increasing Tsub will reduce temperature gradient and therefore wafer warpage.
- Max Tsub is constrained by dopant deactivation and potential TED

Optimization By Integration Schemes

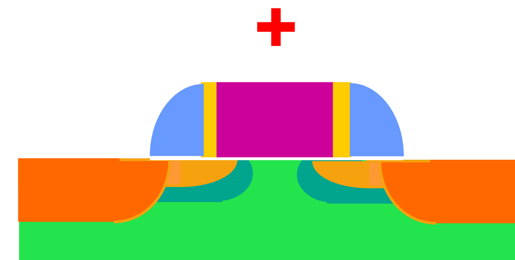
2 Step LSA Insertion
(T. Yamamoto et. al, IEDM'07)

- SDE & Halo Implant with Co-implant
- LSA (step1): optimum
- Sidewall Formation
- ΣSiGe Formation (PMOS)
- Deep SD Implant
- LSA (step2): optimum
- Spike RTA
- Silicidation



(1) LSA at SDE & halo for channel profile engineering

+



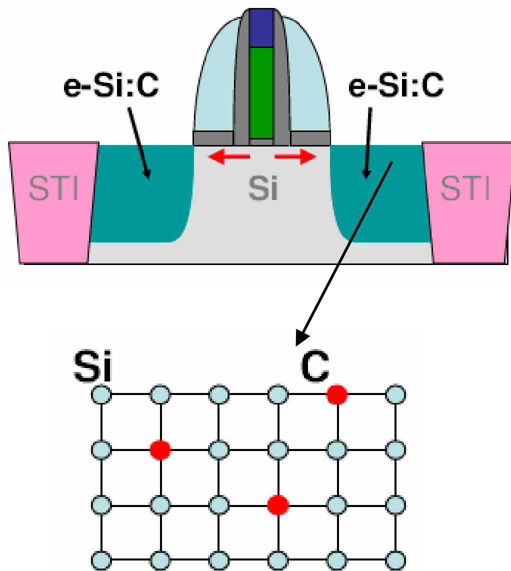
(2) LSA at deep S/D before RTA

2 step LSA before RTA reduces annealing T requirement but NMOS performance may not be optimal.

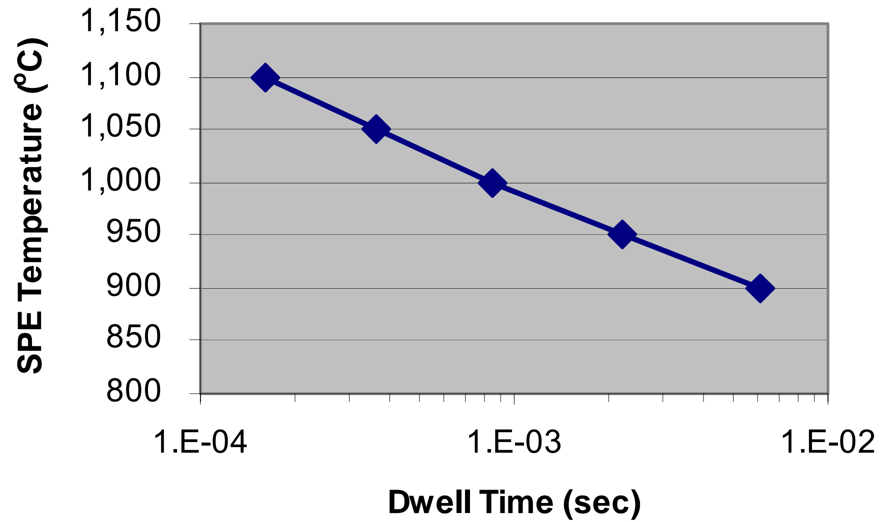
Laser Annealing For Strain Engineering

LSA For Embedded SiC NMOS

Need substitional C for embedded NMOS tensile strain application

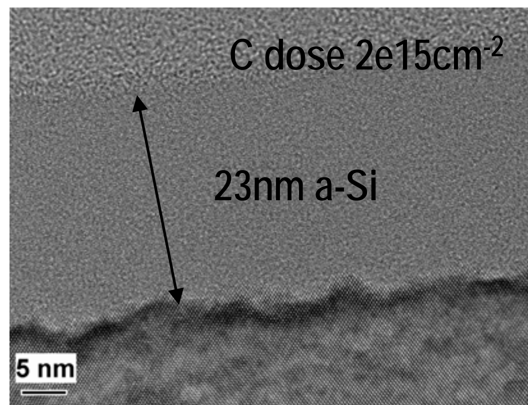


- One promising approach is
  PAI + C impl + SPE
- LSA enables high temperature SPE due to short anneal time.



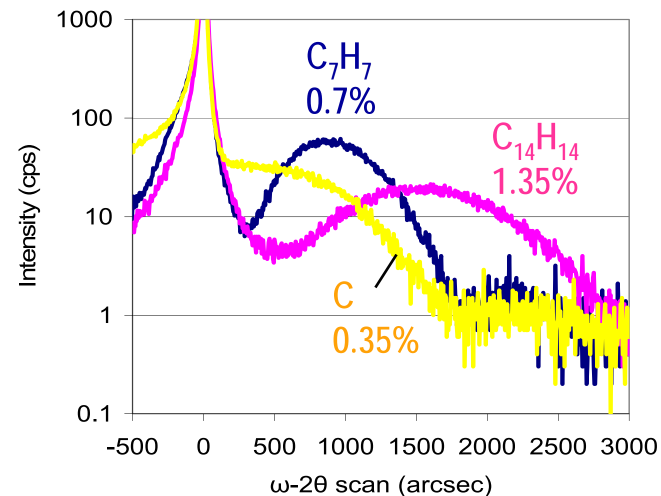
Laser SPE of SiC: Molecular Implant

(a) XTEM After C_7H_7 Implantation



*source: A.L. Fatou, ECS'07

(b) XRD After LSA

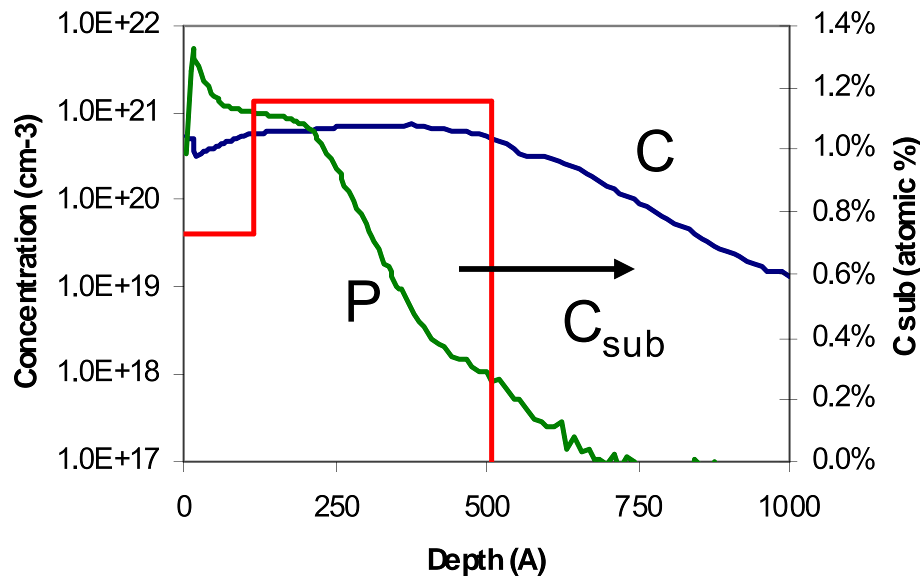


Implant Species	Energy per C Atom (keV)	Substitutional Fraction (at%) (XRD)	Total Fraction (at%) (SIMS)
C	6.6	0.35	0.7
C_7H_7	6.6	0.7	0.7
$C_{14}H_{14}$	3.3	1.35	1.4

Almost 100% of carbon substitutionality can be achieved.

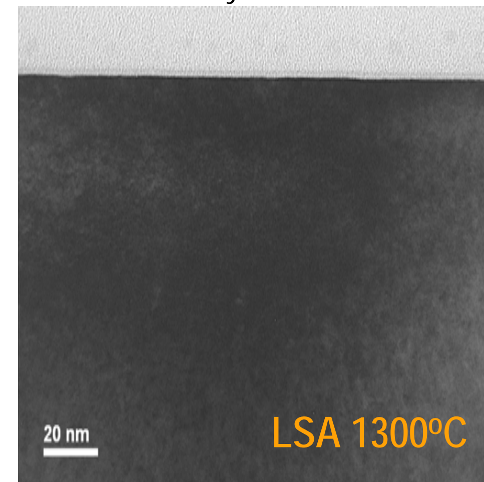
Laser SPE of SiC: Atomic C Implant

C 11keV_1.25e15 cm^{-2} + 5.5keV_4.1e14 cm^{-2} +2.5keV_3.7e14 cm^{-2}
Enhanced amorphization technique
P 7keV_3e15 cm^{-2}



(a) SIMS profiles & C_{sub} from XRD

*source: H. Maynard et al, RTP'08

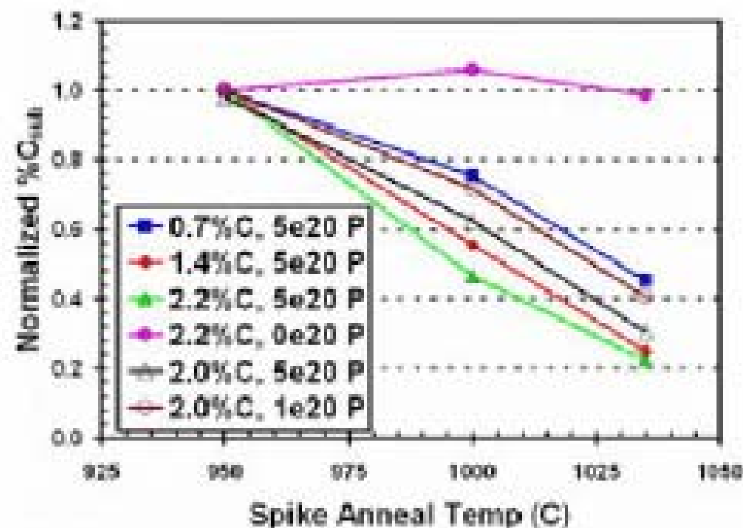


(b) No EOR damage with PR2 after LSA

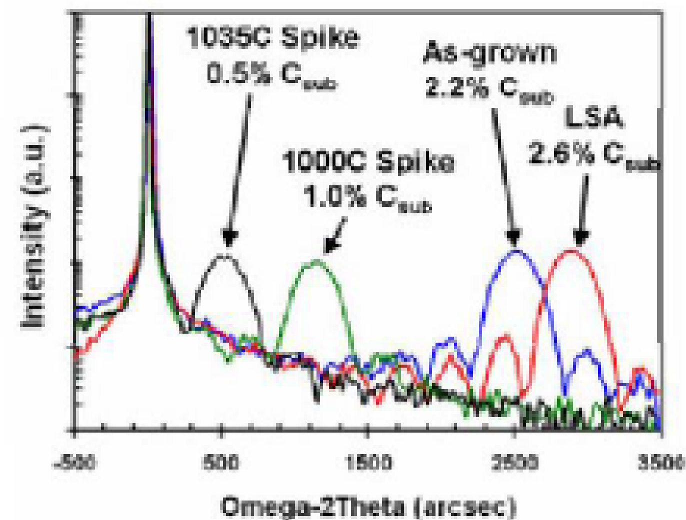
Defect free SiC junction demonstrated.

Post Anneal of SiC Selective Epitaxy

(a) Thermal stability of SiC:P



(b) XRD Spectra



*Source: P. Grudowski et. al. (Freescale),SOI'07

- **RTP above 950°C on SiC epitaxial films can severely degrade C_{sub}.**
- **LSA anneal at 1300°C can improve C_{sub} by converting more interstitial carbon into substitutional.**

Summary

- **Millisecond annealing can induce high transient thermal stress due to large temperature gradient.**
- **CGS technique offers unique full-wafer and patterned wafer capability for characterization of thermal processes**
- **Thermal plastic deformation in SiGe wafers can be reduced by optimizing process parameters and integration schemes. An effective way is to use short dwell time which also improves Rs-Xj scaling.**
- **LSA offers high temperature SPE that is beneficial for both carbon substitutionality and junction activation.**