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W Metallization in a 3-D Memory

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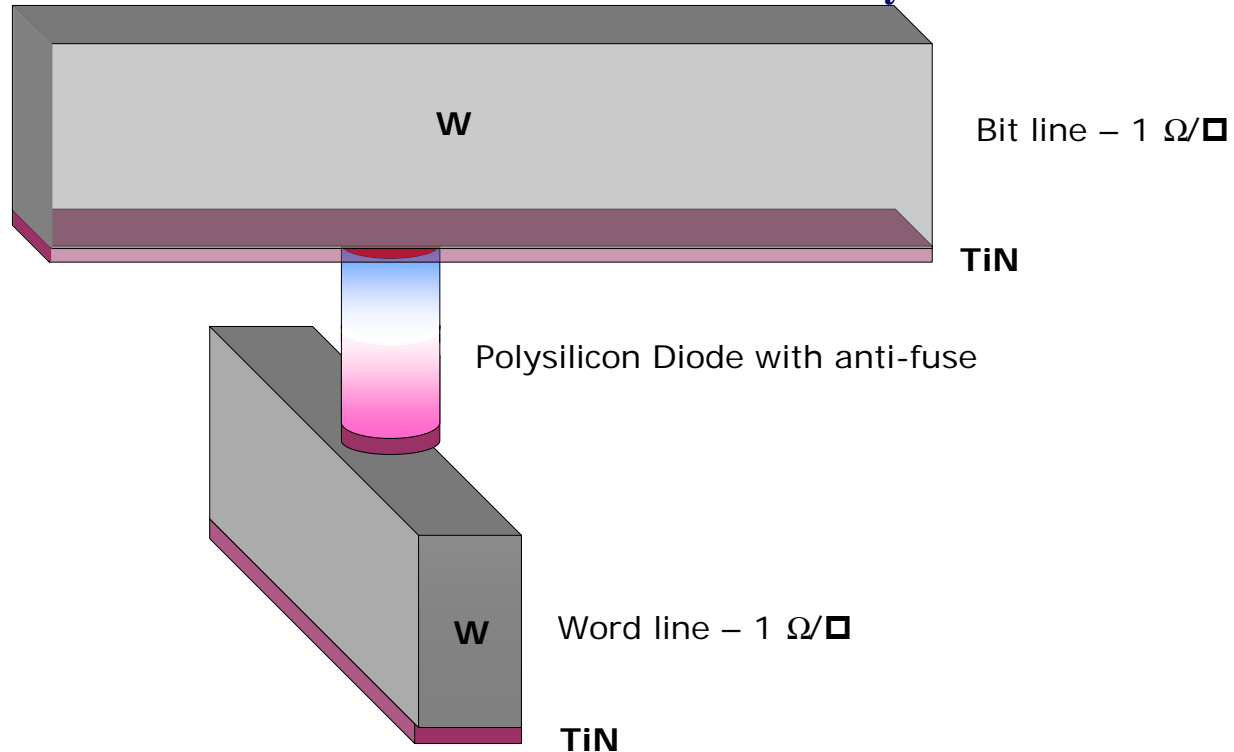
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3-D Memory Cells

- **Matrix memory cells consist of a memory element sandwiched between two conducting wires (wordlines & bitlines).**
- **The memory element is a silicon diode in series with an oxide anti-fuse¹.**
- **Word lines & bitlines are W wires with TiN adhesion/barrier layers**

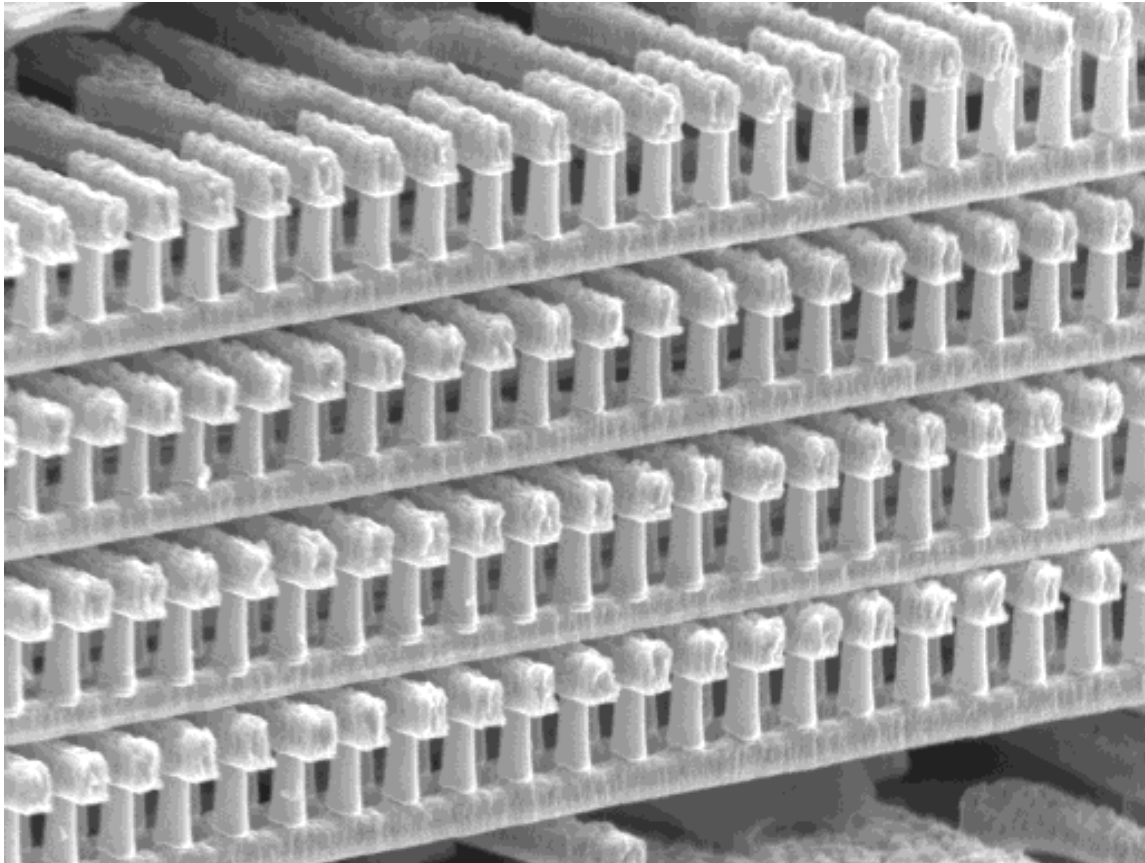


1. S.B.Herner et al., Vertical p-i-n polysilicon diode with antifuse for stackable field programmable ROM, IEEE Electron Device Letters, Vol. 25, 2004, p.271



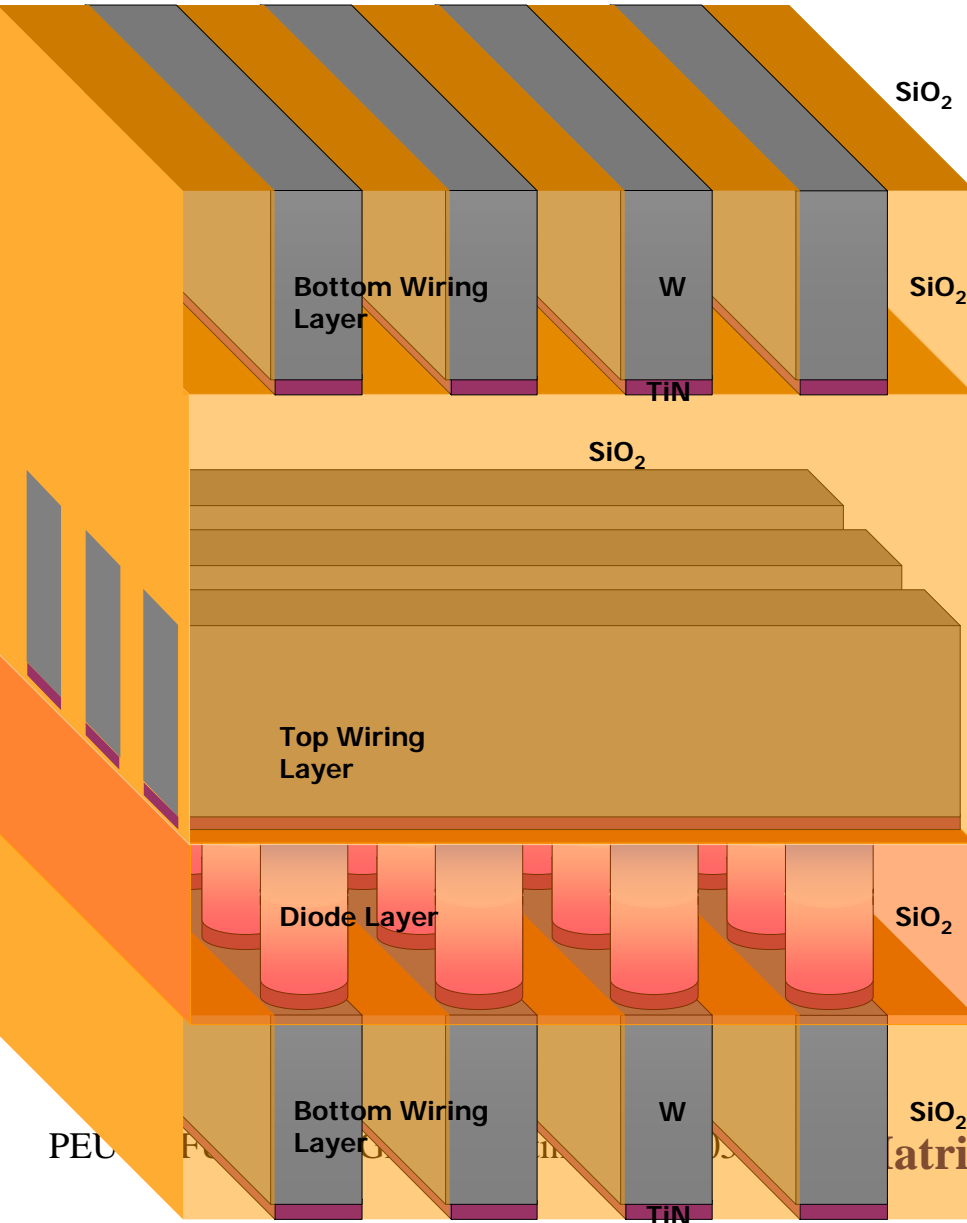
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What is a 3-D Memory?



- **Several memory cells are contacted by a single word line or a bitline.**
- **Each memory layer consists of arrays of memory elements sandwiched between several word lines and bit lines**
- **Memory layers are stacked vertically to achieve higher density (as many as 4 layers).**

3-D Memory Fabrication



- **Matrix 3-D Memory Array Fabrication Process Steps:**
- Deposit Conductor
- Pattern wordlines
- Dielectric Fill
- Planarize and expose top of word lines
- Deposit memory material
- Pattern diodes
- Dielectric fill
- Planarize and expose memory element
- AF formation
- Deposit top conductor
- Pattern bitlines
- Overfill bitlines and planarize

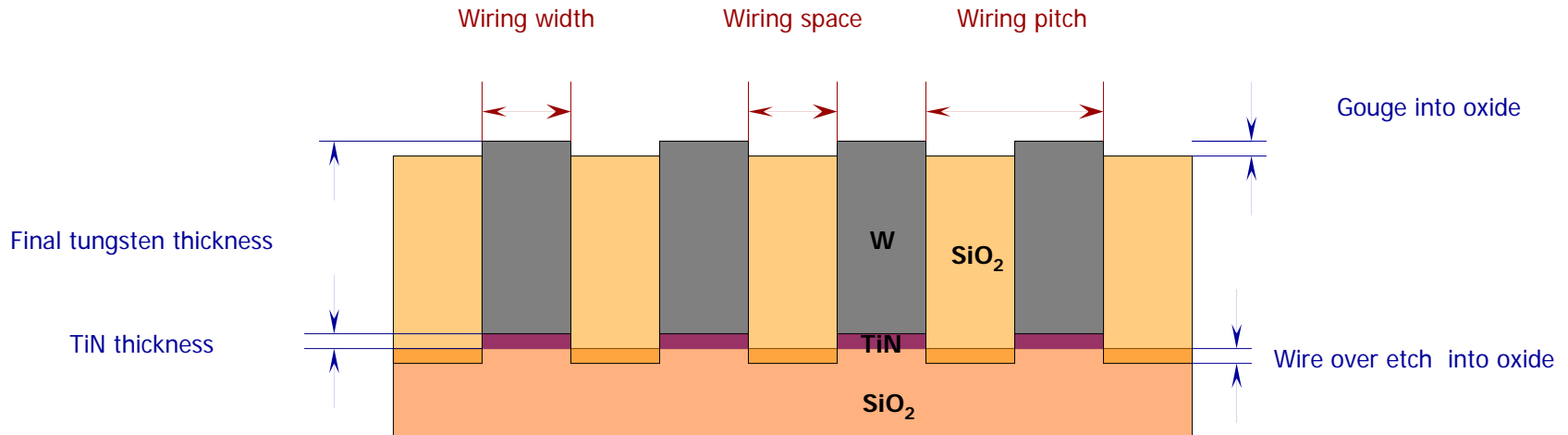
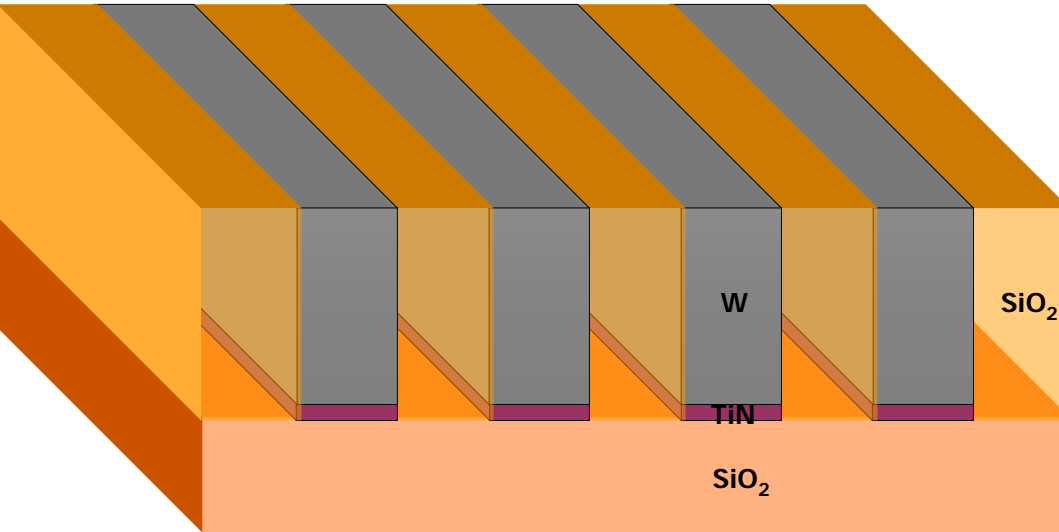
Memory Layer



Wiring Layer Definition

Wiring Layer

- Wires – Tungsten with TiN adhesion layer
- Subtractive patterning (dep, photo, and etch)
- HDP oxide for gap fill
- Oxide CMP or Etchback for planarization (exposes tungsten)





Patterning W Wires

- **Requirements:**

- In our devices, the W is patterned by a subtractive etch process as opposed to a damascene process.
- Device requirements demand a sheet resistance of $\sim 1\Omega/\square$ for the W lines since each W wire contacts several memory elements.
- The W thickness should be over 1500\AA in order to meet these requirements.
- This thickness is 2-3 times the thickness of W used in gate applications at the same technology node.
- Typically, selectivity to resist during W etch is very poor (typically less than 1) with typical SF_6 or NF_3 based etch chemistries².
- As the device dimensions shrink, the incoming photo resist thickness shrinks³ (3:1 aspect ratio) to enable the required photo process window.
- In this presentation we are going to talk about W etch optimization and the changes to process flow with shrinking CDs.

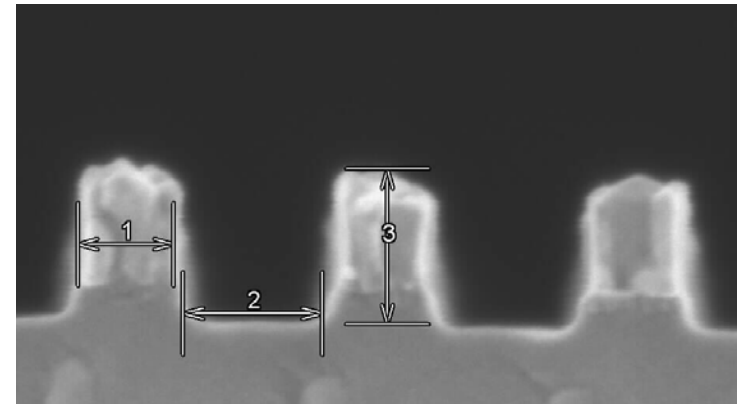
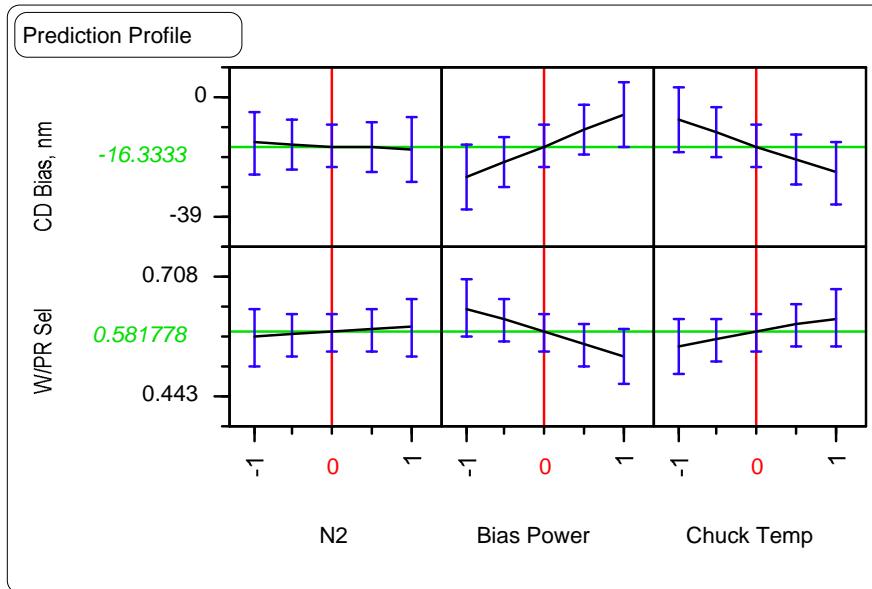
2. B. Kim et al., Use of neural networks to model low-temperature tungsten etch characteristics in high density plasma, J. Vac. Sci. Technol. A, Vol. 18, 2000, p.417

3. Resist Requirements – Near-term Updated, International Technology Roadmap for Semiconductors, 2004 Update, Lithography, Table 78a



Patterning W Wires with 248nm Resist

- For 0.13 μm generation, the incoming photo resist thickness is about 4000 \AA .
- In order to etch the W/TiN stack, a selectivity of over 0.65:1 to PR is required.
- With increase in bias power and decrease in chuck temperature, CD bias decreases (from negative to close to about zero bias), but the PR selectivity also decreases.
- An optimized point with $\sim -10\text{nm}$ CD bias and sufficient PR selectivity was found for the 0.15 and 0.13 μm generations.



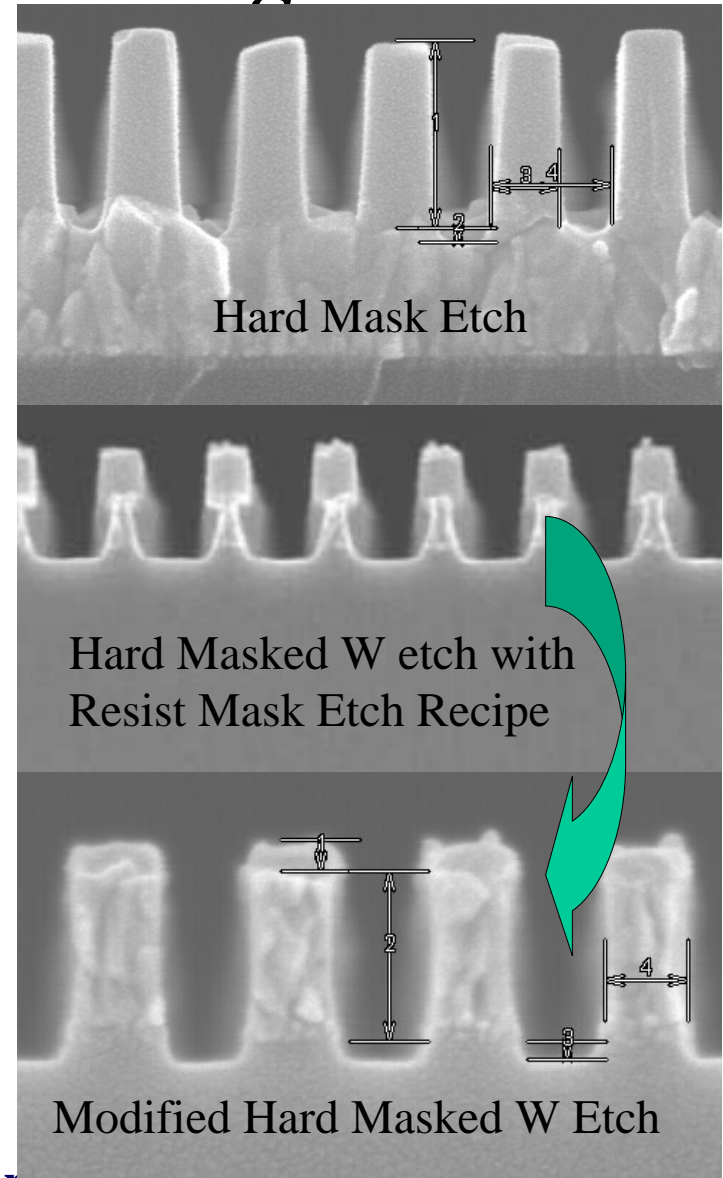
Patterning W Wires with ArF Photo

- For the sub $0.1\mu\text{m}$ generations, the photo processes use 193nm ArF resist which has even poorer etch resistance.
- In addition, the resist thickness goes down to $\sim 2500\text{\AA}$ or below.
- Without the thickness of W going down, we require a hard mask to pattern W.
- The thickness of hard mask is limited by two factors.
 - i) Should be thick enough to withstand the etch and provide sufficient process margin.
 - ii) Hard mask remaining must be thin enough to become an insignificant factor in the aspect ratio for subsequent gap-fill.
 - iii) Easily integrated into the process flow.
- Oxide was chosen as the hard mask for our application since it was readily available and had reasonable etch selectivity to W.
- The oxide hard mask is etched and cleaned before the W is patterned.



W Hard-mask Patterning

- With the hard masked process, it becomes even more critical to have a CD bias that is not negative since a negative bias of W underneath the mask would lead to an undercut profile making the gap-fill process challenging (see picture below).
- The profile undercut was eliminated by:
 - decreasing the fluorine precursor/ N_2 ratio,
 - decreasing chuck temperature, and
 - increasing the bias power.





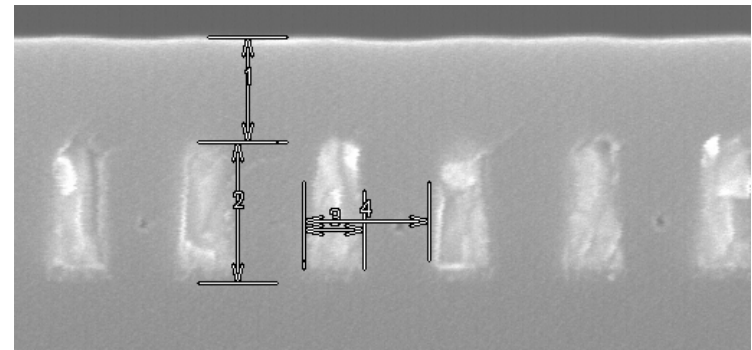
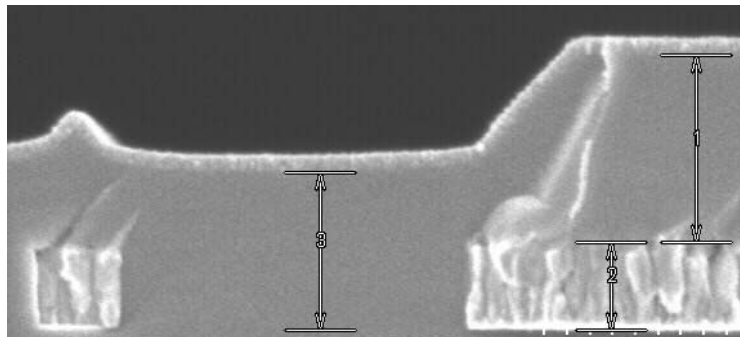
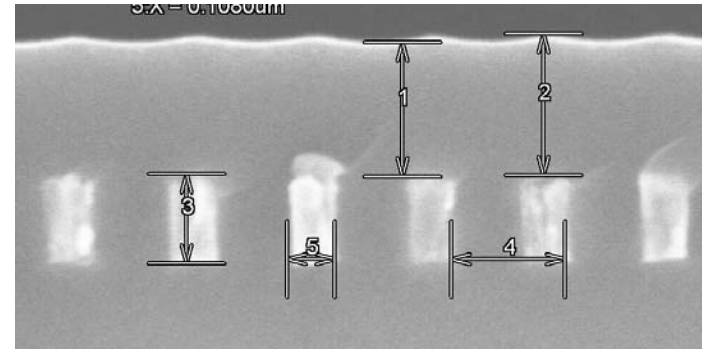
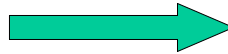
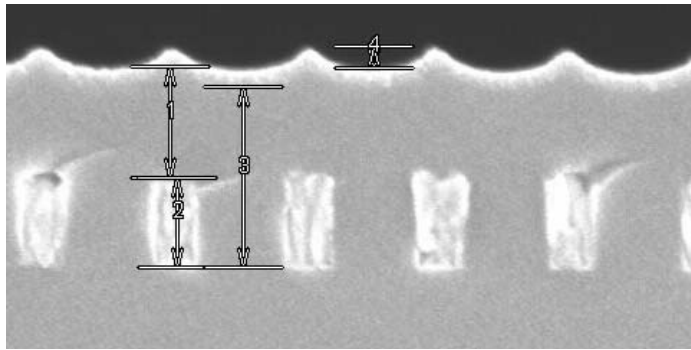
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W Wire Isolation

HDP gap-fill (dielectric isolation) process is self planarizing.

In other words, the oxide surface becomes planar with overfill.

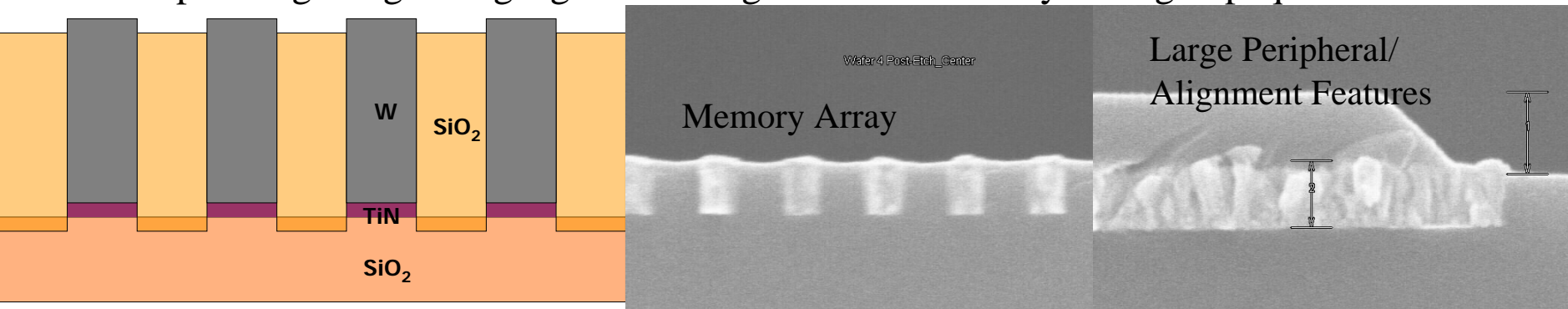
The thickness required for planarization (removal of hats) depend on the etch/ dep ratio during gapfill and feature size.





W Wire Planarization

- **Process Options for Exposing the Top of W Wires:**
 - a) After the dielectric gapfill (wire isolation), the oxide on top of the W wires can be removed by either a CMP process (Chemical Mechanical Polishing)
 - b) As an alternative, a plasma etchback process can be chosen for exposing the top of the W wires when the arrays are planarized by HDP oxide deposition.
- Main difference between the CMP and plasma etchback process is in the amount of oxide remaining over large features.
- In the case of plasma etchback process, the oxide thickness on large features when the array features are exposed is essentially equal to the difference in the incoming HDP oxide thickness between the array and the large features, while it is much less in the case of CMP.
- Preserving the topography on large features such as alignment and overlay marks is helpful in getting strong signals for alignment and overlay through opaque material.



Etch-back Process for Exposing W wires.



Summary

- Matrix 3-D memory architecture involves stacking several memory layers.
- Each memory layer consist of several memory elements (made of a poly silicon diode and an antifuse) sandwiched between word lines and bitlines.
- The process flow involves sequential deposition, patterning fill and exposure of word lines, diodes and bitlines.
- W is used as a wiring material and is patterned using a subtractive plasma etch process.
- Bias power, chuck temperature and fluorine precursor to N₂ ratio were used to optimize the process for both resist masked and hard masked process.
- A CMP or an etchback process can be utilized to expose the active elements since the HDP gapfill process is self-planarizing.