Roll-to-Roll Manufacturing of Electronics on Flexible Substrates Using Self-Aligned Imprint Lithography

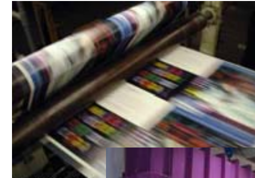
Ohseung Kwon, Marcia Almanza-Workman, Alison Chaiken, Robert Cobene, Richard Elder, Bob Garcia, Warren Jackson, Mehrban Jam, Albert Jeans, Han-Jun Kim, Hao Luo, Ping Mei, Craig Perlov, Carl Taussig

Hewlett-Packard Company, Palo Alto, CA, USA

Frank Jeffrey, Kelly Beacom, Steve Braymen, Jason Hauschildt, Don Larson,

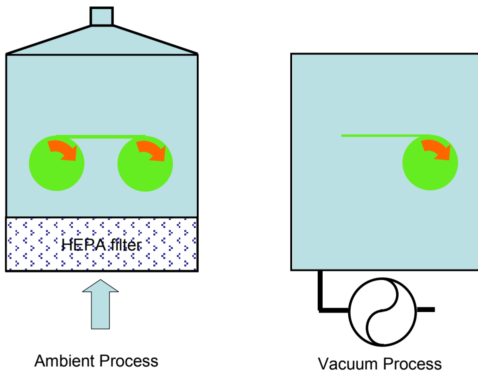
PowerFilm Solar, Ames, IA, USA

Roll-to-Roll (R2R) Fabrication of Electronics



If you want lemonade;
start with lemons

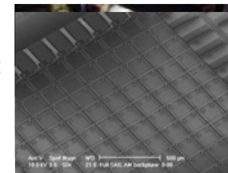
The web rolled on the core is its own clean room



Overview

- Why SAIL?
- SAIL process modules:
  - Thin film deposition
  - Imprinting
  - Self-aligned etching
- SAIL flexible AM backplane:
  - a-Si R2R TFTs & arrays on plastic substrate
- Summary

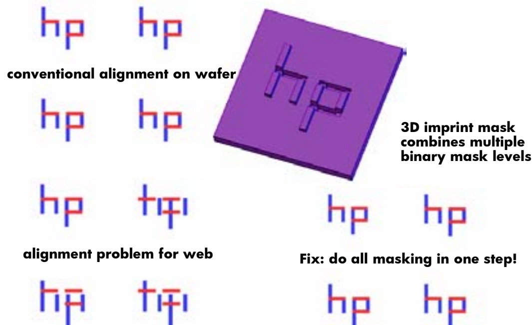
R2R processing is a key enabler for high throughput, low cost production of large area, flexible electronics!



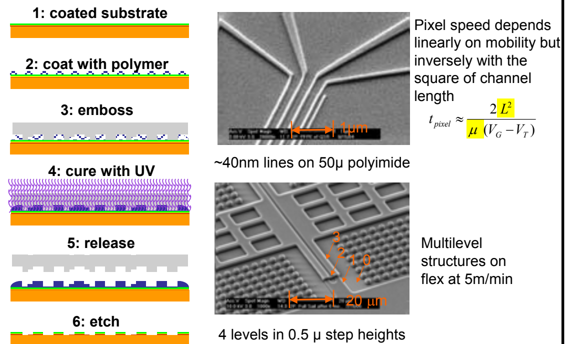
R2R fabricated SAIL TFT array

The Big Problem:

Patterning & Aligning on a Flexible Substrate



Basic Imprint Lithography Process



~40nm lines on 50μ polyimide

4 levels in 0.5 μ step heights

Pixel speed depends linearly on mobility but inversely with the square of channel length

$$t_{pixel} \approx \frac{2L^2}{\mu(V_G - V_T)}$$

Multilevel structures on flex at 5m/min

Imprint Lithography:
The Best Choice for R2R Patterning

	photolithography	imprint lithography	inkjet
Throughput	moderate: limited by step & repeat / stitching	high: > 5 meters/min	low
Resolution	limited by substrate flatness ~10μ	100nm demonstrated	>10μ
Materials	PECVD Si, Si_3N_4, SiO_2, vacuum deposited metal, many others	PECVD Si, Si_3N_4, SiO_2, vacuum deposited metal, many others	must be jettable
Alignment of multiple levels	Difficult or Impossible due to web's dimensional instability	Self-alignment of multiple patterning layers	Requires secondary sensor

What is SAIL?

3 sequential processes on the flexible web

Deposition	Imprinting	Self-aligned etching
Vacuum deposition of metals, dielectrics, and semiconductors	Multiple mask levels imprinted as single 3-D structure	Patterning with wet and dry processes based on the imprint mask

Fully R2R

SAIL: Self-Aligned Imprint Lithography

Photolithography

Multiple masking and alignment steps required

Different mask used to pattern each layer

Process induced distortion of 200ppm results in 20μ misalignment over 10cm

SAIL

SAIL encodes multiple patterns and alignments into thickness modulations of a monolithic masking structure

Single mask used to pattern all the layers multiple times

No misalignment because mask distorts with substrate

R2R SAIL process flow is very different from conventional batch

deposition: Vacuum deposition of metals, dielectrics, & semiconductors

imprint: Multiple mask levels imprinted as single 3D structure

etch: Patterning completed w/ wet & dry processes

Conventional Photo-Lith: deposit, spin resist, align/expose, develop, etch, strip/clean

SAIL: deposit, imprint, etch, etch mask

SAIL solves alignment problem & saves money

Multiple photoresist applications dominate photolithography process materials costs

Backplane materials costs for R2R photolith & SAIL

Cost of Patterning

cost per ft²

Photolithography

SAIL

R2R SAIL

R2R photolith (AGI)

Why SAIL?

Objective: R2R flexible AM backplanes

- Large Area
- High Resolution
- Inexpensive

Advantages of SAIL

- End-to-end R2R process
  High Throughput, Enhanced Uniformity, Less Cleanroom Requirement
- Sub-micron interlayer alignment on meter-scale substrates
  Sub-micron Patterning Resolution, Faster Response Time
- Opportunity for Lowest Possible Process Cost
  No Photolithography during Production, Equipment Scaled with Width not Area

SAIL process: Deposition

Unique deposition processes have resulted from volume manufacturing of a-Si solar cells

Demanding military applications have proved ruggedness

•Device grade SiN_x and SiO_x added to existing processes for metal and semiconductor deposition.
•New plasma etching added for patterning

SAIL process: Deposition

Sputtered Cr
PECVD n+ μ-xstal Si
PECVD a-Si:H
PECVD Si nitride
PECVD Si dioxide
Sputtered Al
50 μm Kapton Polyimide Substrate

•R2R deposition requires different strategies for SiN_x/a-Si interface than batch process

• In-line uniformity enhances with R2R due to steady state process

• SAIL enables in-line deposition of full TFT stacks in the same vacuum chamber providing clean interfaces without expensive cleaning steps

• Taking advantage of the 1μm channel lengths provided by SAIL requires improved n+ contacts

SAIL process: Imprinting

Imprinted web

Imprinting roller with elastomeric stamp

Imprinted web

→ **40 nm** line width

→**sub-micron** features with **4 levels** and **5:1 aspect ratio**

Coating Station
Imprinting Station
Supply
Take-Up

House-built R2R coating & imprinting machine

(Throughput rate = **5 m/min**)

SAIL process: Etching

Then undercut to remove from under thinnest parts of mask

Individual SAIL TFT device

Imprint polymer
S&D metal Cr
n+ uC Si contact
a-Si semiconductor
SiNx dielectric
Gate metal Al
Polymer substrate

R2R Plasma Etching Technology

Requirements
- •Uniformity: process margin
- •Anisotropy: minimize CD loss in etch mask

Challenges
- •Batch endpoint detection methods won't work for a steady-state R2R process
- •Achieving anisotropy with a grounded web is difficult

Wet etcher: acid-based etching of metals

- 1/3 m wide web, 1.5m/min max web speed; sidelay control
- two separate selectable process chemistries: currently Cr and Al
- immersion based system; multiple rinse steps
- 200C dry / anneal tunnel
- HEPA filtered enclosure better than class 100

Front-side contact
Etch
Rinse 1
Rinse 2
Dryer

Wet Etch Layout

SAIL TFTs

Kapton (Polyimide) Substrate

Gate (Al)

Channel (a-Si)

S/D (Cr)

- 4 level bottom-gate a-Si TFTs (equivalent to 3 masks)
- Deposition, imprinting and dry etching with R2R
- S/D areas are separated from the gate area by wet etching

SAIL backplane: array 'unit cell' TFT

5μ

Undercut etch patterns bottom metal to isolate gate contact beneath S/D metal

10μ

50μ

Perfect alignment maintained throughout 30m long web

Substrate (polyimide)

Gate (Al)

Channel (a-Si)

50μ

S/D (Cr)

SAIL backplane

- 4 level mask
- W/L = 40/2μ TFTs

Dual data line array

Arrays designed with two separate data lines connected to each pixel for full testing on probe station with or without integration with front plane

SAIL backplane: array 'unit cell'
Undercut used to pattern bottom metal

Top metal

Si stack

Dielectric bilayer

Undercut bottom metal

1μ

Substrate (polyimide)

Acc.V Spot Magn 8.00 kV 3.0 15000x Full-SAIL TFT 1 μm

'Full-SAIL' TFT arrays:
undercut of bottom metal isolates gate lines

Fully processed array showing crossover of gate lines by data lines

Array with data lines and TFT stack etched away to reveal how undercut has isolated the gate lines

Performance of Full-SAIL a-Si TFTs

Full SAIL TFTs with thinner dielectrics have greatly improved performance

- on-off ratio > 10^7
- 100μA on-current
- mobility from linear portion of transfer curve as high as 0.8 $cm^2/V/S$
- near linear scaling of I_{on} vs 1/L to L~2μm

Mobility [cm²/V/S]: 1.E 1, 1.E 0, 1.E-1, 1.E-2, 1.E-3

Channel Length [μm]: 1.E 0, 1.E 1, 1.E 2

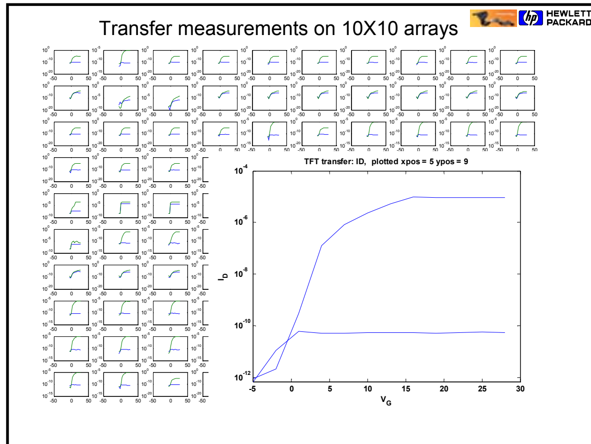
W=100um Vsd=10.1V

Isd/(W/L) (A): 1.E-05 … 1.E-14

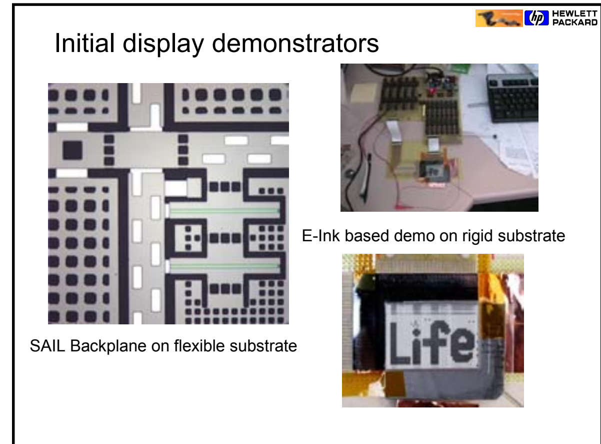
Vg(V): -10, 0, 10, 20, 30, 40

W [μm]	L [μm]
100.0	1.0
100.0	2.0
100.0	5.0
100.0	10.0
100.0	20.0
100.0	50.0
100.0	100.0

Transfer measurements on 10X10 arrays



Initial display demonstrators

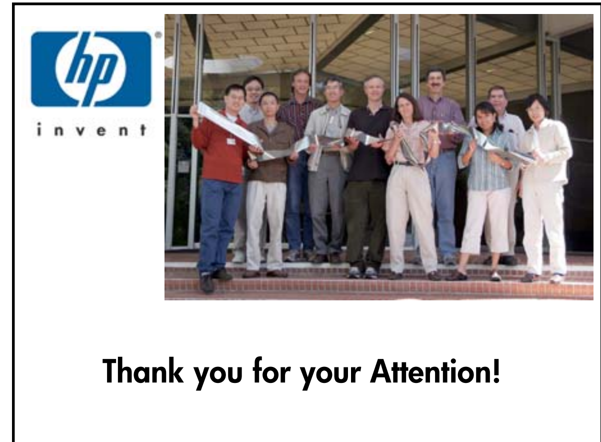


SAIL Backplane on flexible substrate

E-Ink based demo on rigid substrate

Summary

- R2R processing is a key enabler for high throughput & low cost production of large area AM flexible displays
- Self-Aligned Imprint Lithography (SAIL) is an end-to-end R2R process, and enables high precision interlayer alignment and resolution
- Manufacturability of SAIL TFTs and AM backplanes has been demonstrated on the plastic substrate
- TFT stack deposition, imprinting steps, and etching steps are achieved with the R2R environment



Thank you for your Attention!