

# HiK/MG Gate Stack Issues and Landscape

Steven Hung



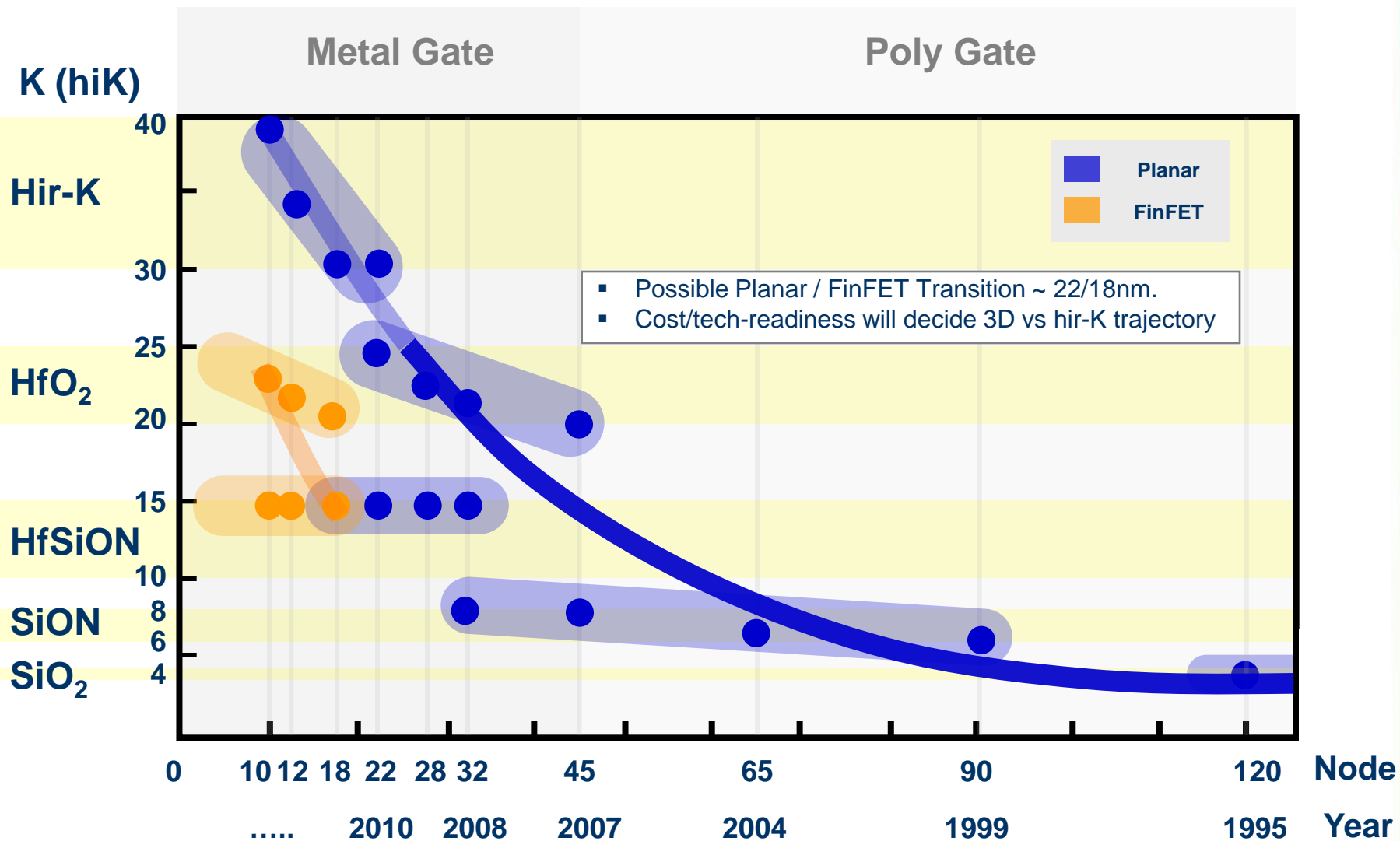
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# Outline



- The K-evolution
- Integration Landscape Overview
- Scaling trend and Limitation
- The Fundamental Gate Stack Material Issues

# Evolution of K-scaling

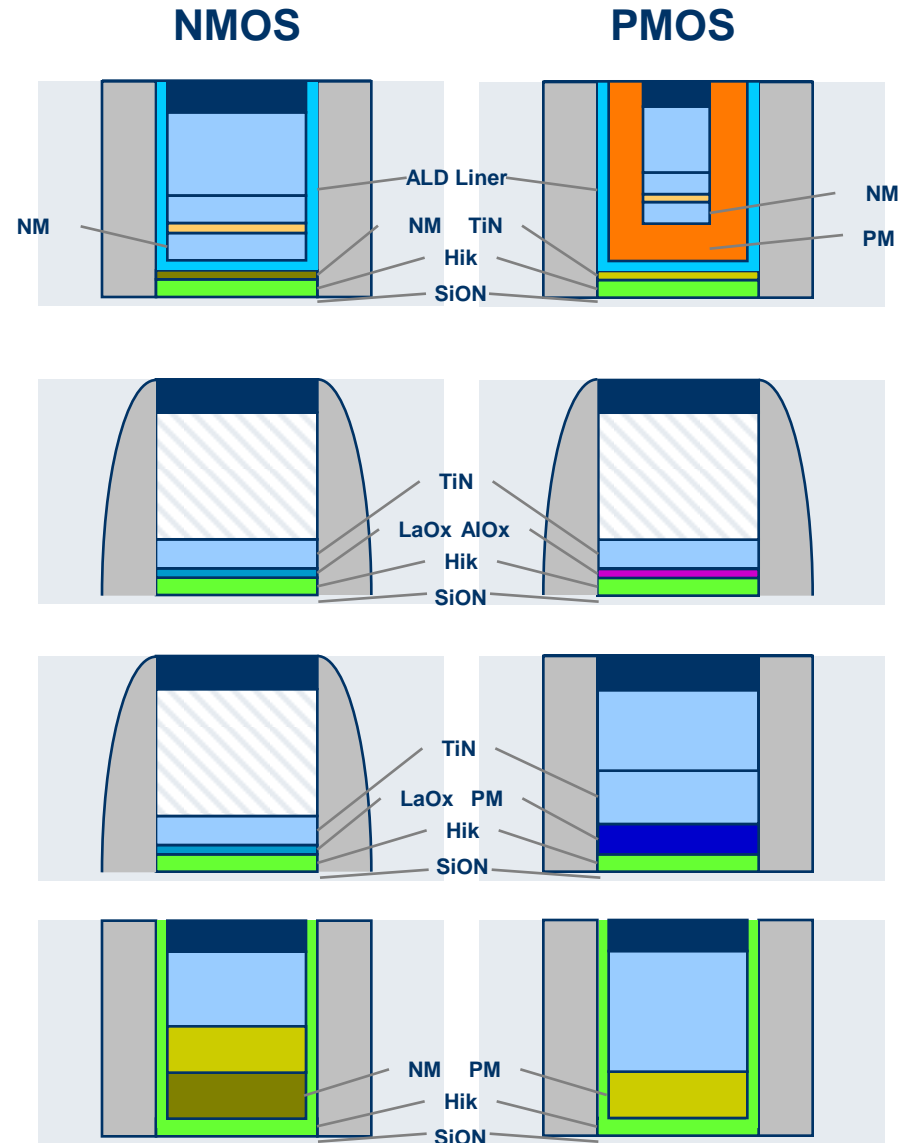




# Overall Landscape on HiK/MG

# General Landscape

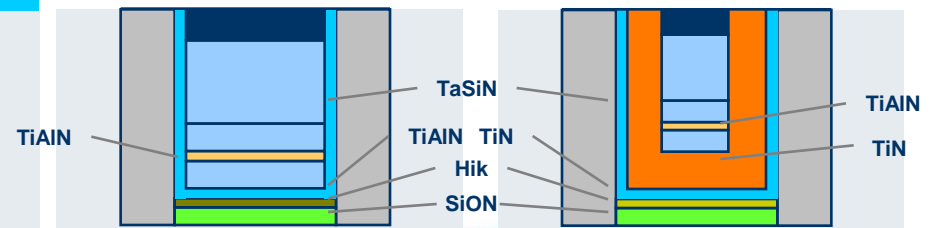
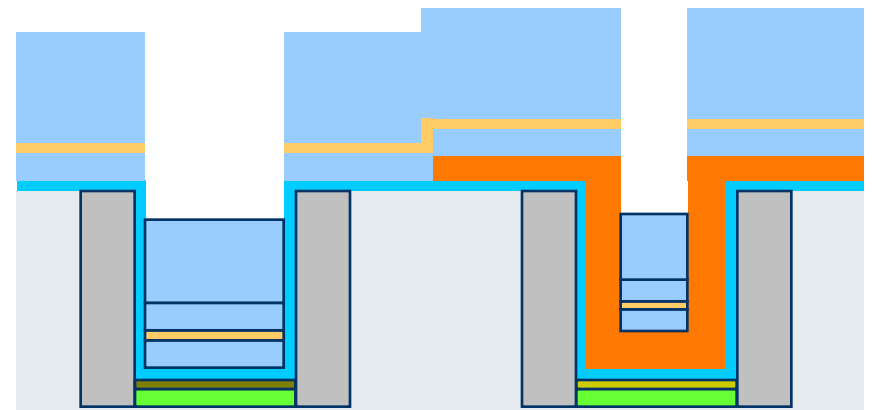
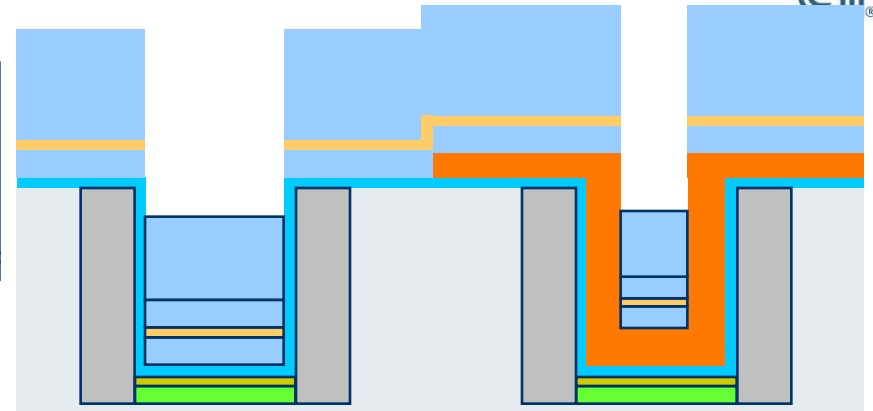
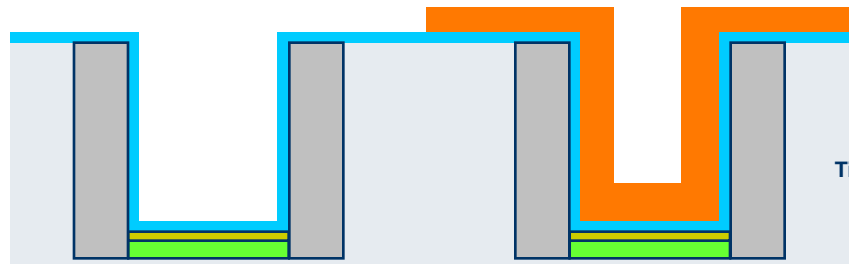
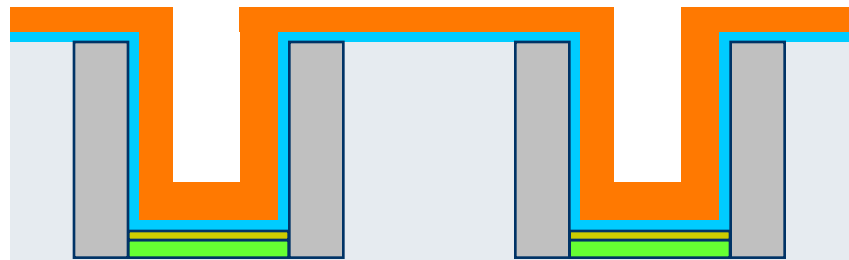
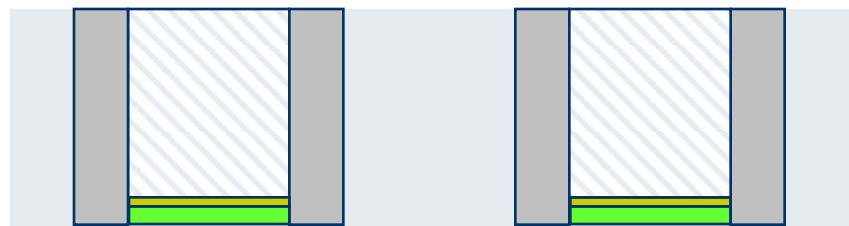
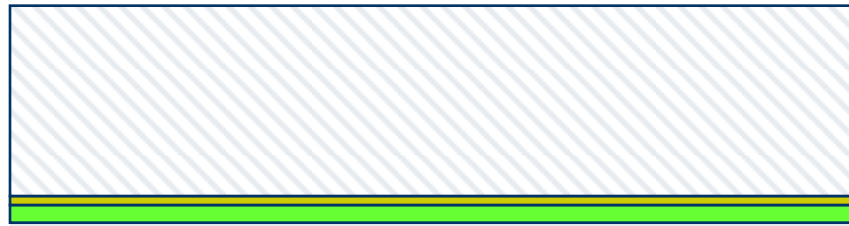
Integration	Process Flow
<b>HiK F + MG L</b>	<ul style="list-style-type: none"> <li>Base Ox + HiK + TiN + Poly + Gate Etch</li> <li>S/D formation + spike</li> <li>CMP + poly strip</li> <li>ALD liner + P-metal</li> <li>NMOS: P-metal wet etch</li> <li>N-metal + Al fill + reflow</li> <li>Al CMP</li> </ul>
<b>GF</b>	<ul style="list-style-type: none"> <li>Base Ox + HiK</li> <li>Dep AlOx / Midgap Metal</li> <li>Etch of AlOx / MG on NMOS</li> <li>Dep LaOx / Midgap Metal</li> <li>Etch of LaOx / MG on PMOS</li> <li>Poly + Gate Etch + S/D formation + spike</li> </ul>
<b>Hybrid GF (N) GL (P)</b>	<ul style="list-style-type: none"> <li>Base Ox + HiK</li> <li>Dep LaOx / Midgap Metal</li> <li>Etch of LaOx / MG on PMOS</li> <li>Poly + Gate Etch + S/D formation + spike</li> <li>Poly strip on PMOS</li> <li>P-metal dep + Al fill + reflow</li> <li>CMP</li> </ul>
<b>Pure GL</b>	<ul style="list-style-type: none"> <li>Dummy dielectric + Poly + Gate Etch</li> <li>S/D formation + spike</li> <li>CMP + poly strip</li> <li>Base Ox + HiK + N-metal dep</li> <li>N-metal etch from PMOS</li> <li>P-metal dep + metal fill</li> <li>CMP</li> </ul>



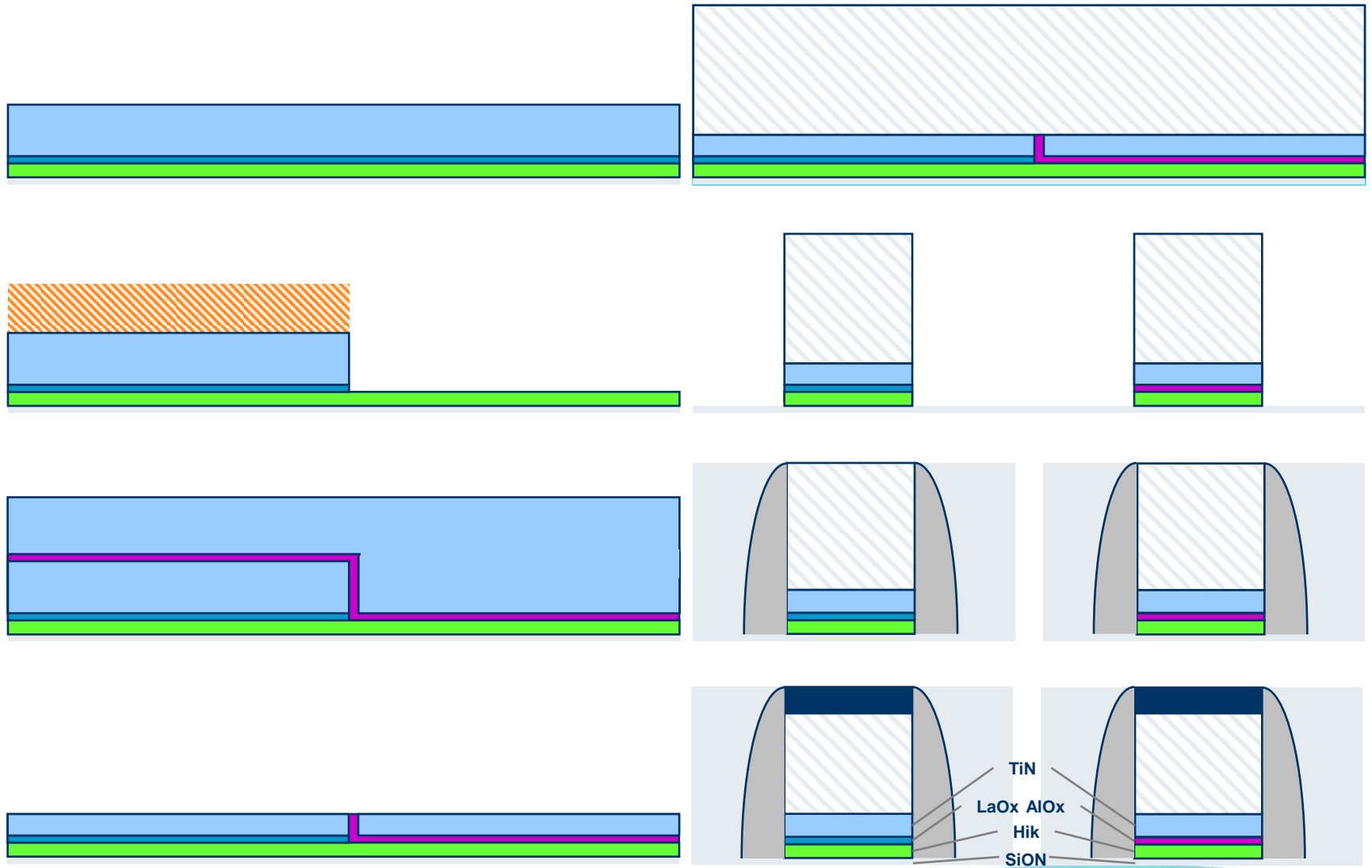
# HiK First, MG Last

NMOS

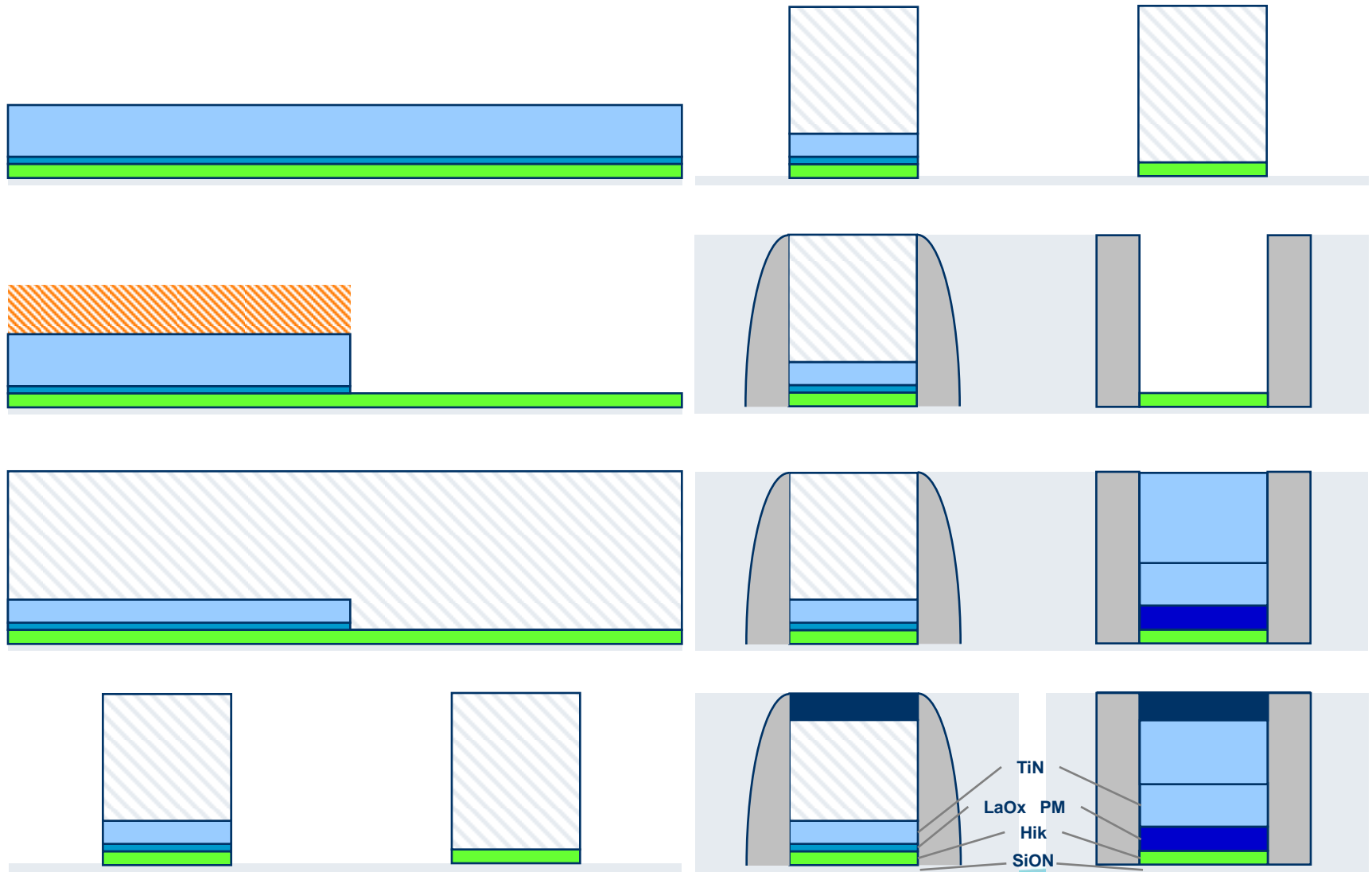
PMOS



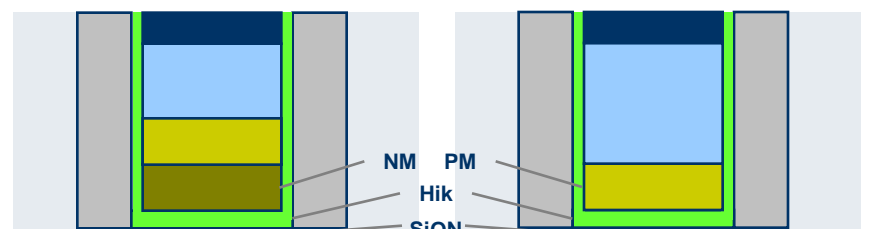
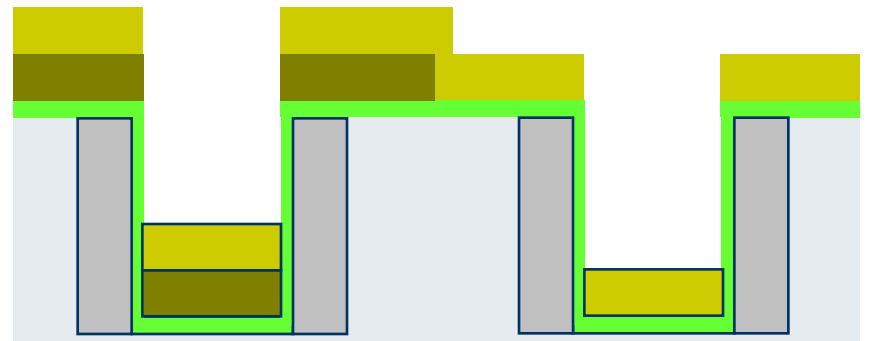
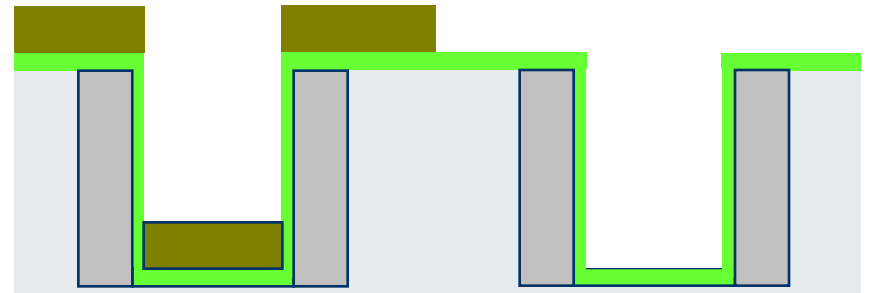
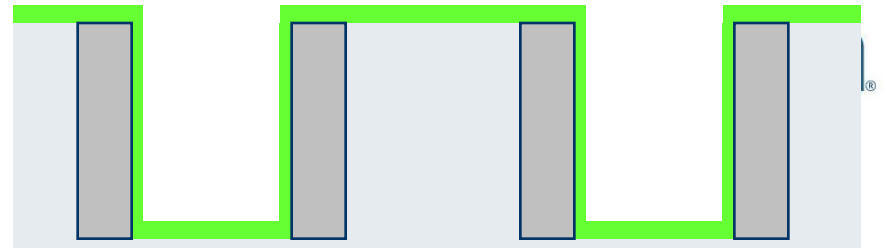
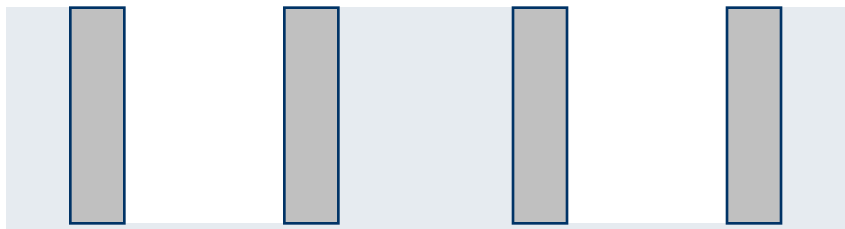
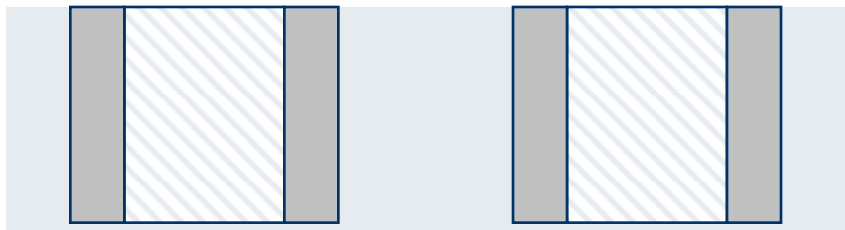
# Gate First (GF)



# GF (NMOS) / GL (PMOS)



# Gate Last (GL)



# Issues and Challenges for Hik/MG Stack



- Base Oxide
  - Development of sub-10A higher-K Box for EOT scaling
  - SiON: Proper N-dose and profile to maximize K and minimize EOT
- Hik
  - Morphology stability for GF & GL applications
  - Process control to minimize Oxygen vacancy ( $V_o$ )
  - Post deposition passivation for Oxygen vacancy suppression
- Capping layer
  - Deposition sequence and etch selectivity
  - Insufficient  $V_t$  adjustment on PMOS with AlOx (requires  $\Delta V_t > 300\text{mV}$ )
  - Mobility degradation due to over diffusion of La and Al species
  - Stringent uniformity requirement for  $V_t$  control WIW & WTW
- MG
  - Deposition process control to prevent damage to cap layer & hiK
  - Gap fill and overhang issue for both N and P devices

# Trends and Solutions for 32nm and beyond

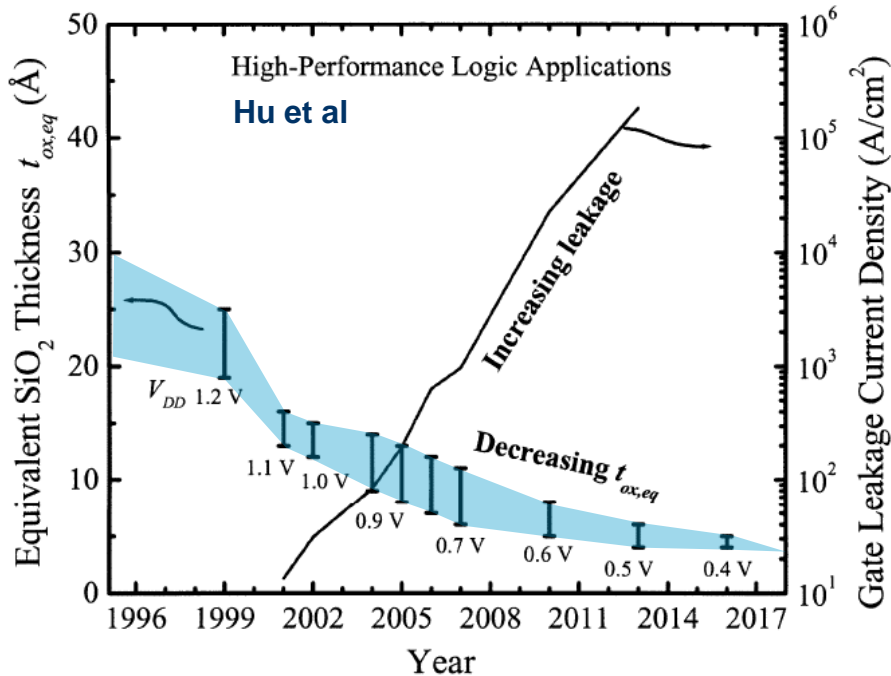


- Base Oxide
  - Use of SiON for aggressive EOT scaling in HP application
  - Utilize densified Base Ox to prevent trace element penetration into channel
- HiK
  - Use of optimal ALD seq and temp for complete & secure in-film bonding
  - Post deposition anneal to suppress Vo formation (ie; NH3 PDA)
  - Post deposition nitridation for morphology stability and Vo reduction
- Capping layer
  - Possible alternatives for PMOS: MnOx, VOx, TaOx, ZrOx
  - Use of densified Base Ox to prevent La or Al penetration to channel
  - Use of uniform deposition technique / process for Vt control
- MG
  - Low damage deposition to prevent Metal or N diffusion into hiK
  - ALD metal dep for GL or 3D applications

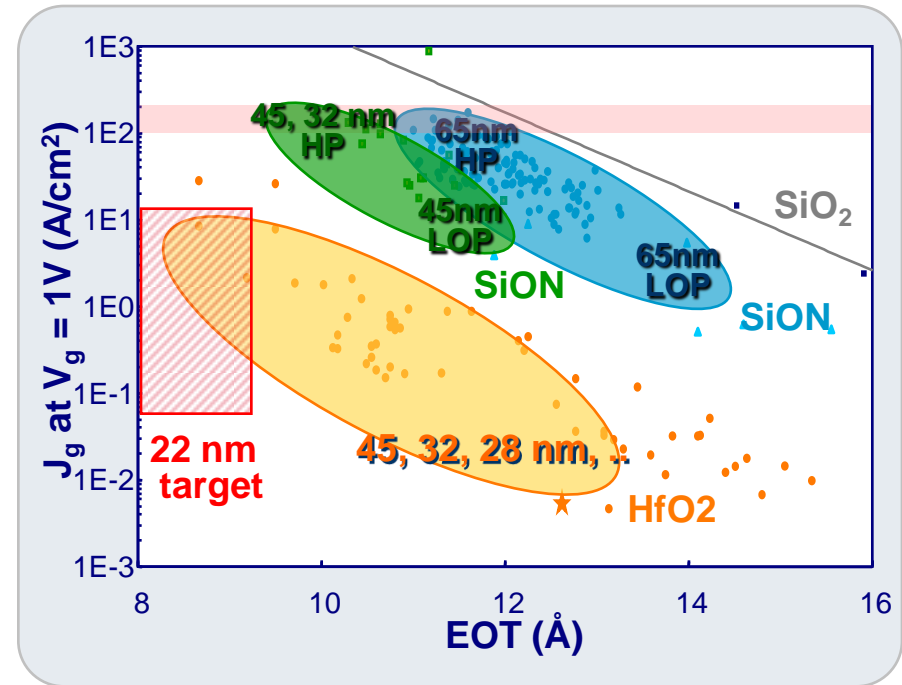


# Fundamental Challenges on HiK/MG Stack

# Evolution of Jg/EOT



IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 50, NO. 4, APRIL 2003

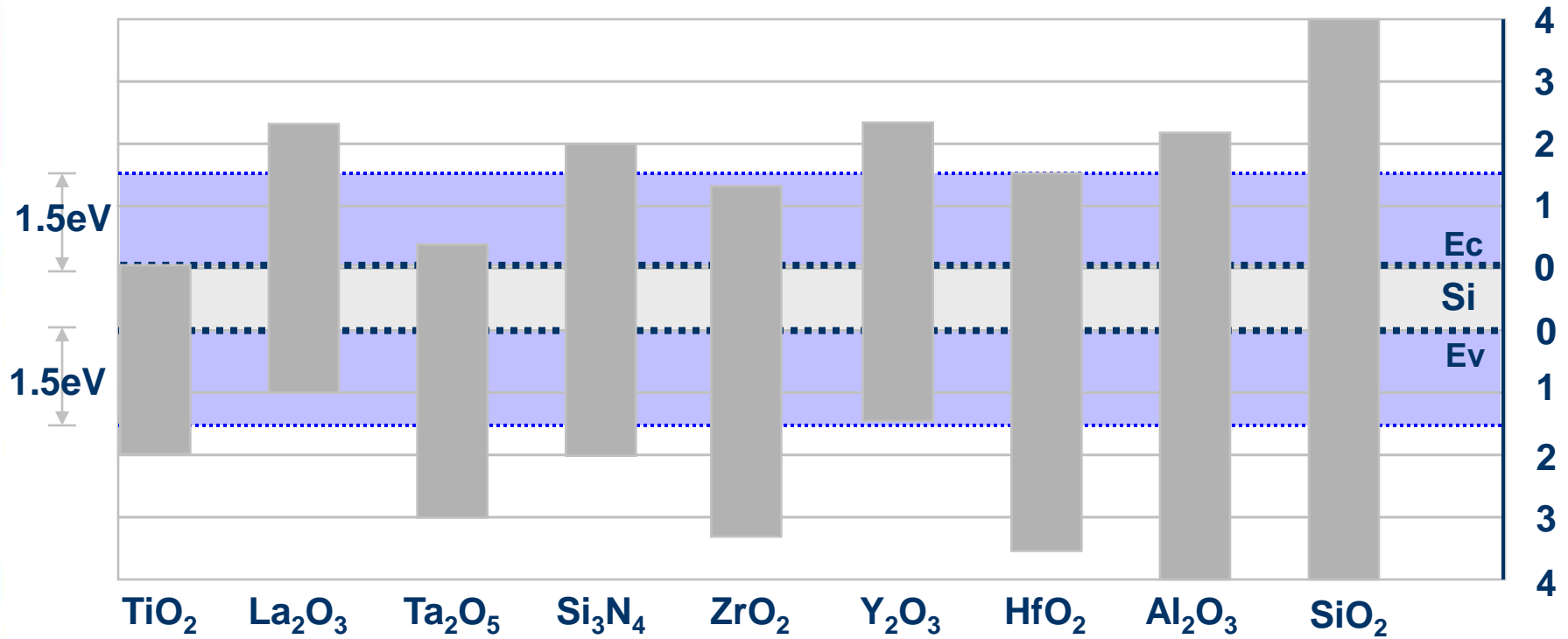


- Scaling limitation of SiON:  $J_g \sim 1E2$  A/cm<sup>2</sup>, EOT  $\sim 10$ Å.
- 100x  $J_g$  reduction from SiON requires new dielectric system.
- Poly depletion forces the use of metal gate for EOT control.

# Scaling Comparison of Various Dielectrics

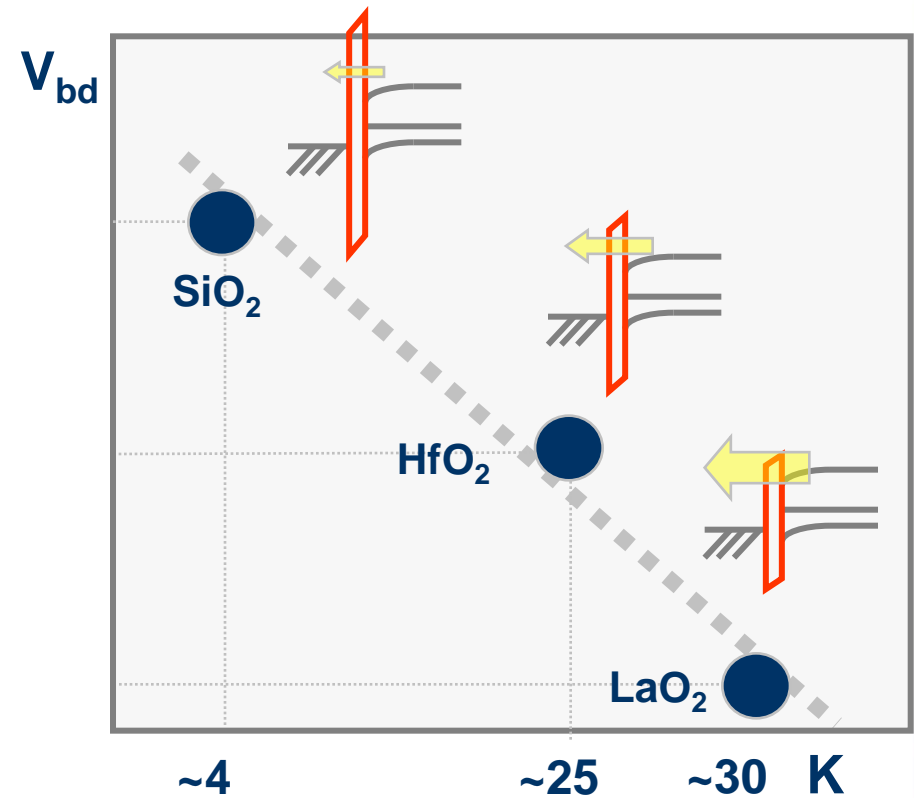
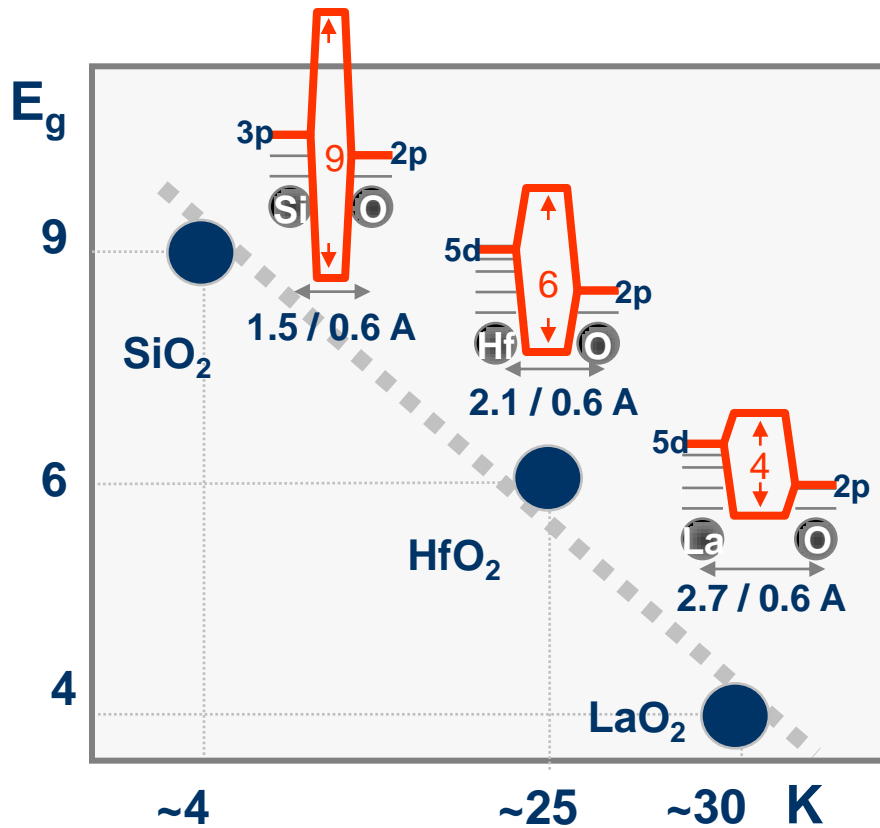


- Barrier height needs at least 1.5 eV for proper leakage suppression.



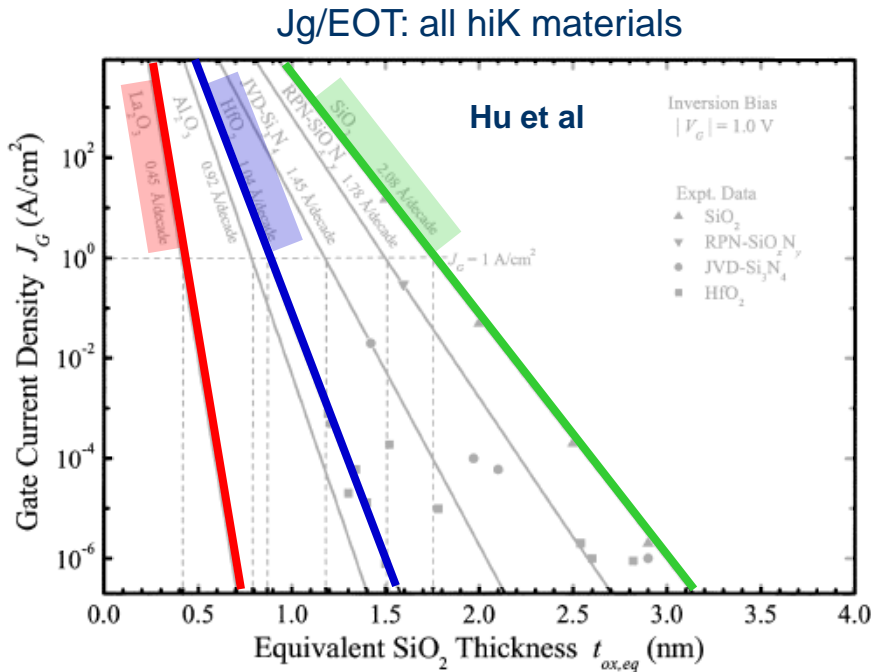
	TiO <sub>2</sub>	La <sub>2</sub> O <sub>3</sub>	Ta <sub>2</sub> O <sub>5</sub>	Si <sub>3</sub> N <sub>4</sub>	ZrO <sub>2</sub>	Y <sub>2</sub> O <sub>3</sub>	HfO <sub>2</sub>	Al <sub>2</sub> O <sub>3</sub>	SiO <sub>2</sub>	
Eg	3	4.3	4.5	5.1	5.4	5.6	6	8.7	9	Eg
$\Delta\Phi_c$	0	2.3	0.4	2	1.4	2.3	1.5	2.1	4	$\Delta\Phi_c$
$\Delta\Phi_v$	2	1	3.1	2.1	3	2.3	3.5	5.6	4	$\Delta\Phi_v$
k	60	30	25	7	30	15	25	9	3.9	k

# Fundamental Conflicts: $E_g$ vs $K$ vs $V_{bd}$

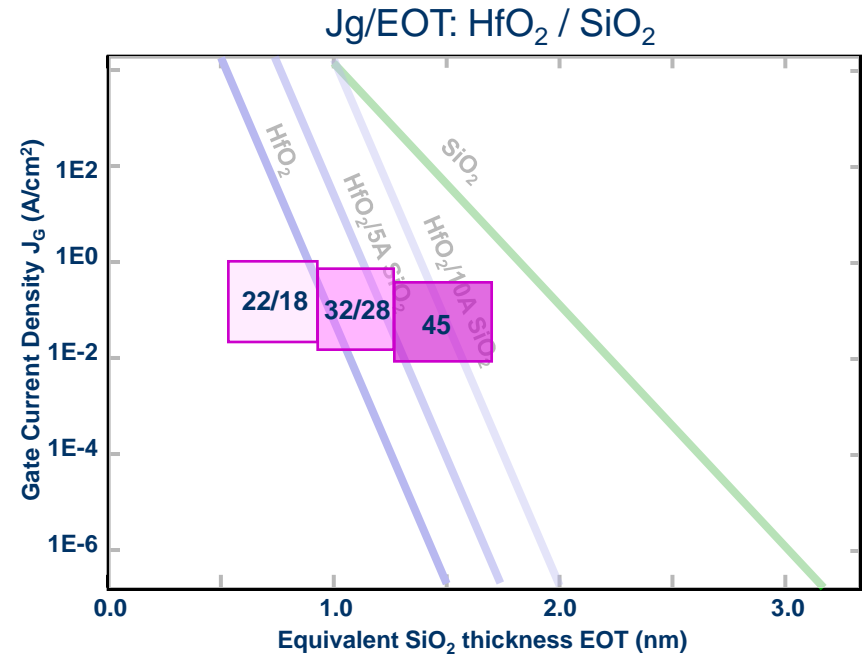


- Small bonding radius (ex  $\text{SiO}_2$ ): Larger  $E_g$ , smaller  $K$ , larger  $V_{bd}$ .
- Large Bonding radius (ex  $\text{LaO}_2$ ): Smaller  $E_g$ , larger  $K$ , smaller  $V_{bd}$ .

# Jg/EOT Scaling Trajectory (w/ & w/o SiO<sub>2</sub>)

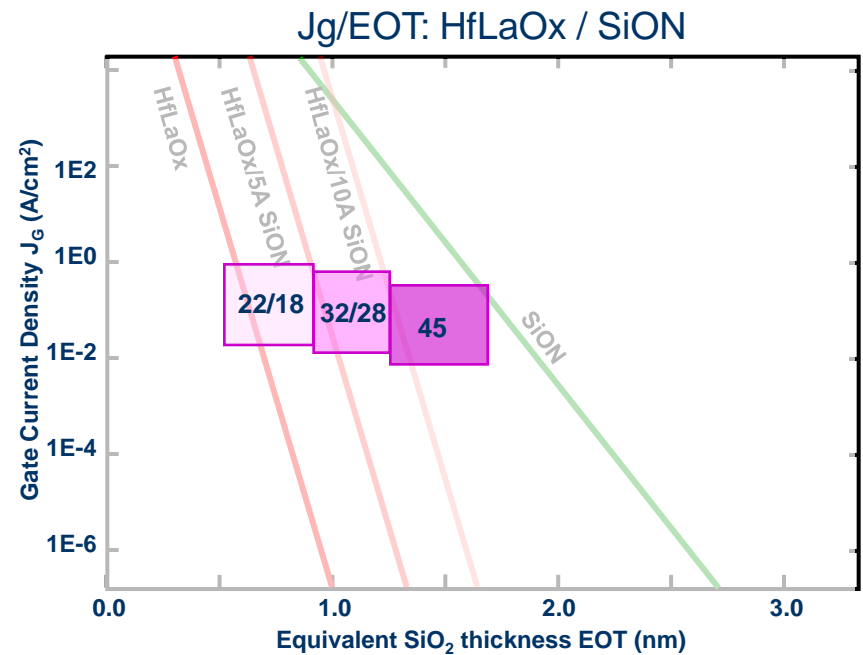
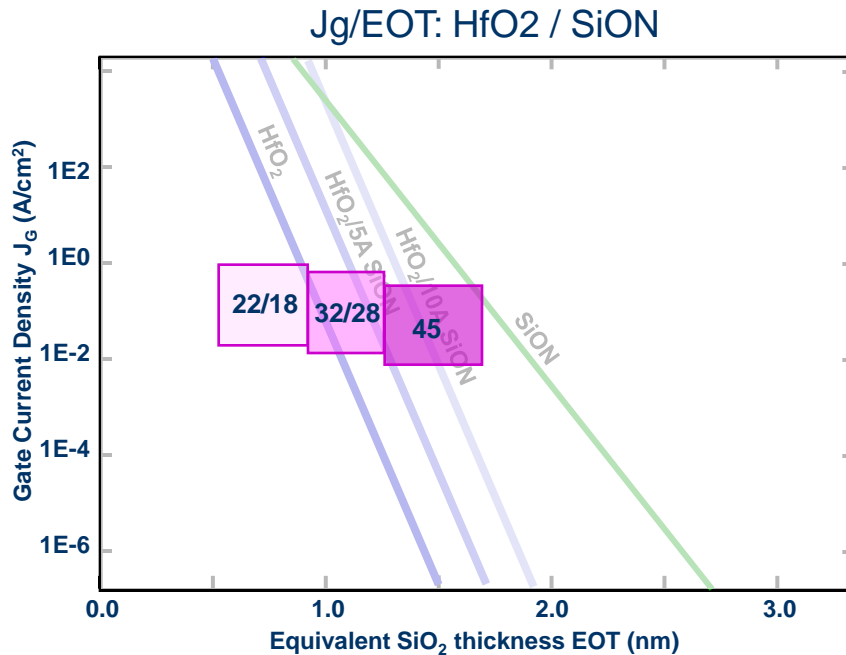


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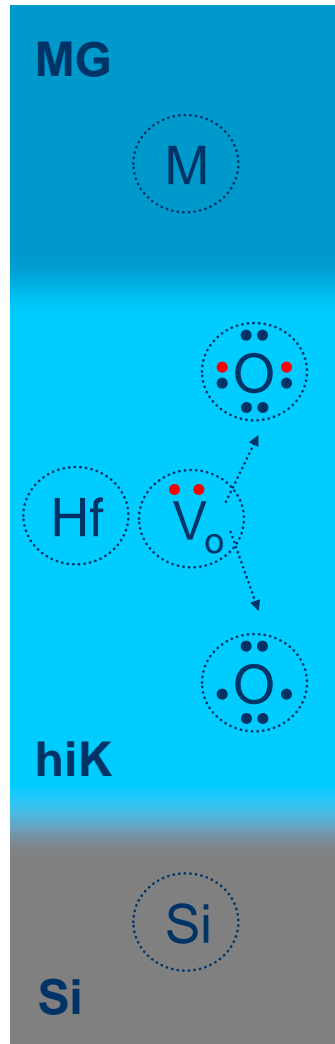
- Without Box, HfO<sub>2</sub> can reach 1/10 (1A/cm<sup>2</sup> J<sub>g</sub> & 10A EOT), but with low  $\mu$ .
- The addition of 5A SiO<sub>2</sub> as Box, HfO<sub>2</sub>/SiO<sub>2</sub> stack can not reach 1/10.
- Box has significant effect on the scalability of HfO<sub>2</sub> for 32nm and beyond.
- Higher-K Box, in combination with HfO<sub>2</sub>, will be needed for 22nm (10<sup>-1/8</sup>).

# Jg/EOT Scaling Trajectory (HfO<sub>2</sub> vs HfLaOx)



- The HfO<sub>2</sub> + SiON can reach 32nm (1/10), but will be hard for 22nm (10<sup>-1/8</sup>).
- Higher-K dielectric (ex: HfLaOx with K ~ 27) can provide additional scaling.
- HfLaOx (as ex.), in combination with SiON, can reach both 10<sup>-1/8</sup> and 10<sup>-3/7</sup>.
- Development of higher-K (>25) will be crucial for sub 22nm applications.

# Evolution of Material and Device Issues



Thermal instability of Hf-O bonding w/r to Si-sub and MG

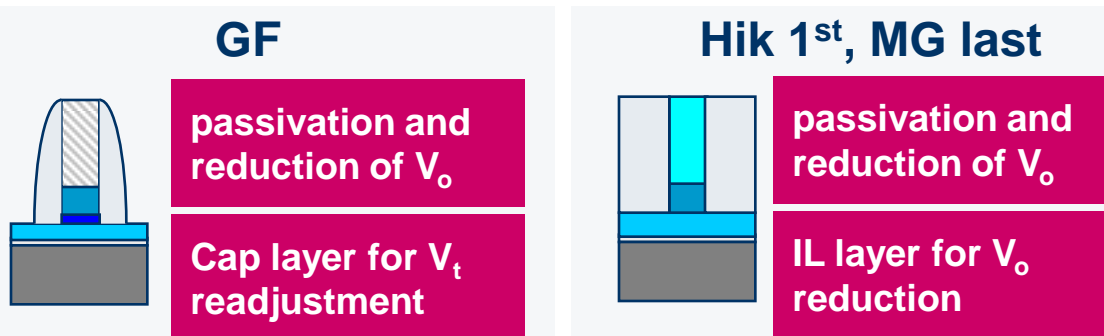
Formation of oxygen vacancy ( $V_o$ ) & Interstitial ( $I_o$ ) in hiK

Redistribution of Ox and formation of dipole

Fundamental material issue

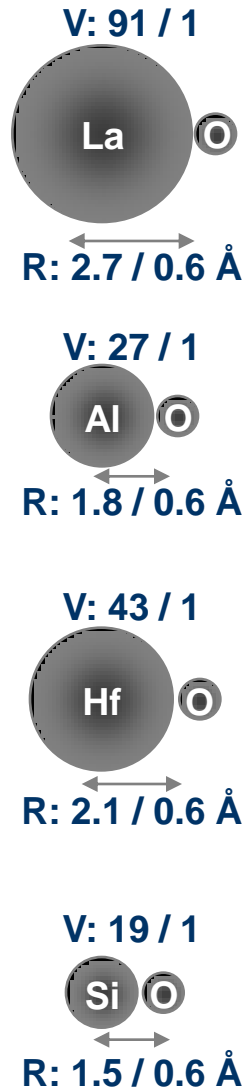
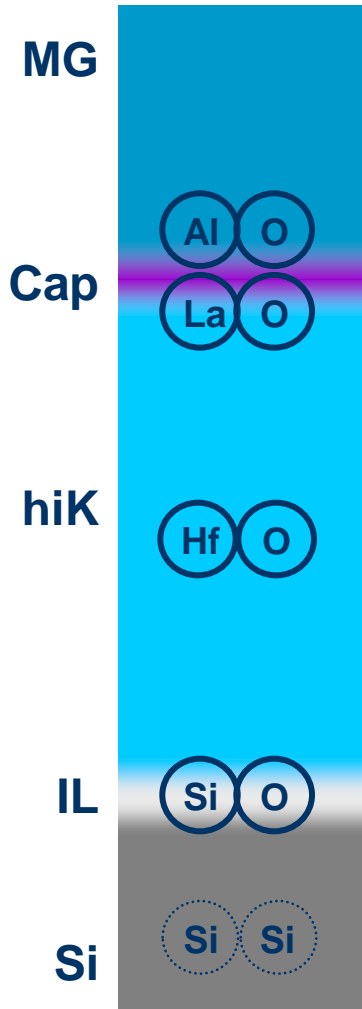
- Fermi /  $V_t$  Pin
- $V_t$  roll off
- Gate leakage
- $V_t$  instability
- Low  $V_{bd}$
- Low  $T_{bd}$

Subsequent device issue



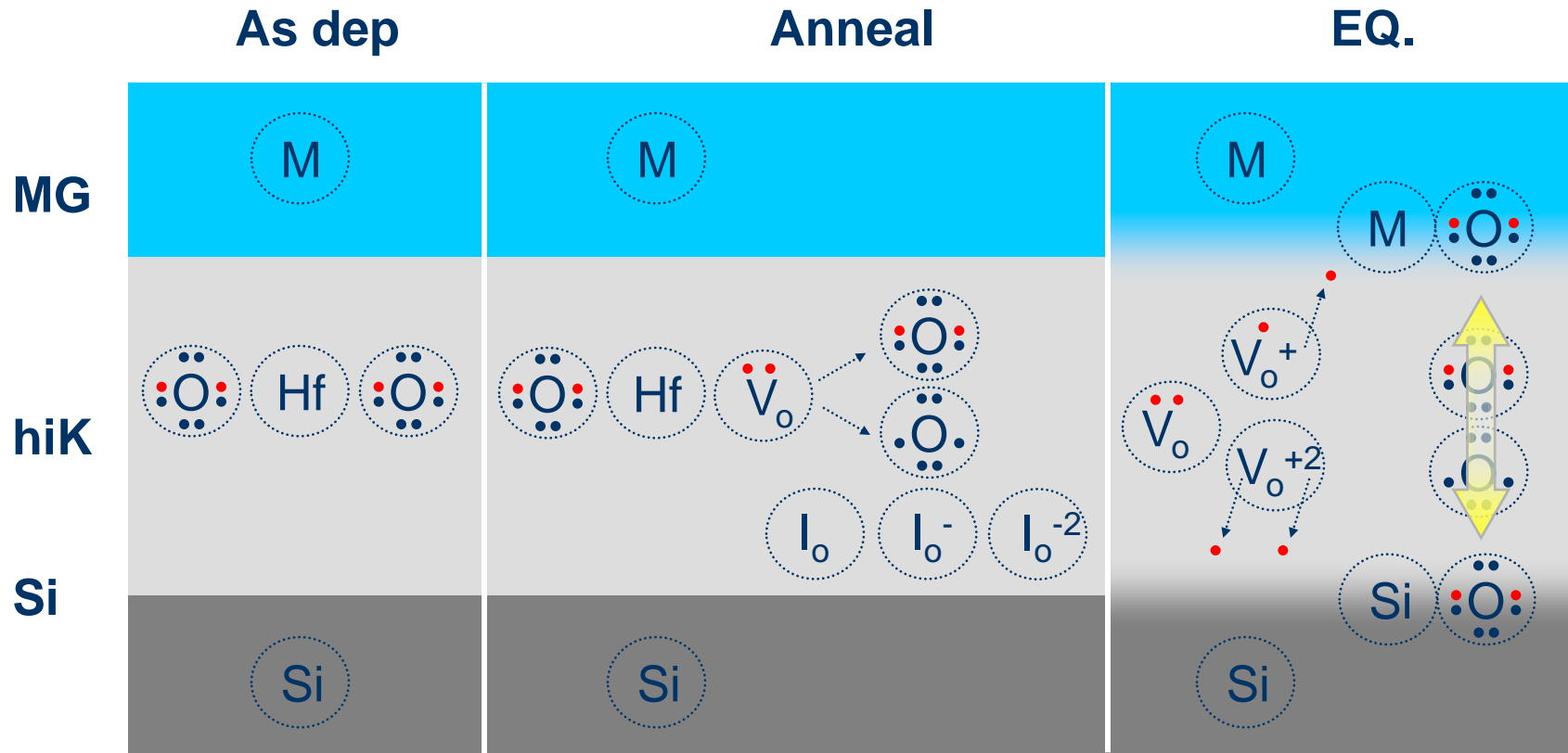
Integration solutions

# Stability of the HiK/MG Stack



Bonding pair	Bonding Energy (KJ/mole)
W-W	666
Ti-N	476
La-O	798
Al-O	501
Hf-N	535
Hf-O	801
O-N	631
Si-N	437
Si-O	799
Si-Si	310

# Evolution and Formation of Vo and Io

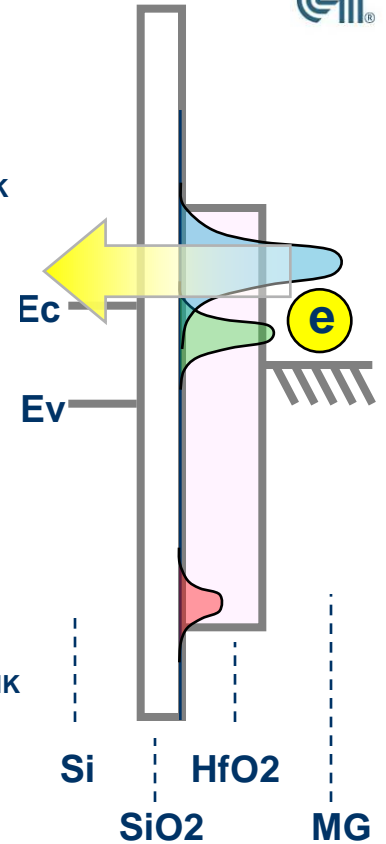
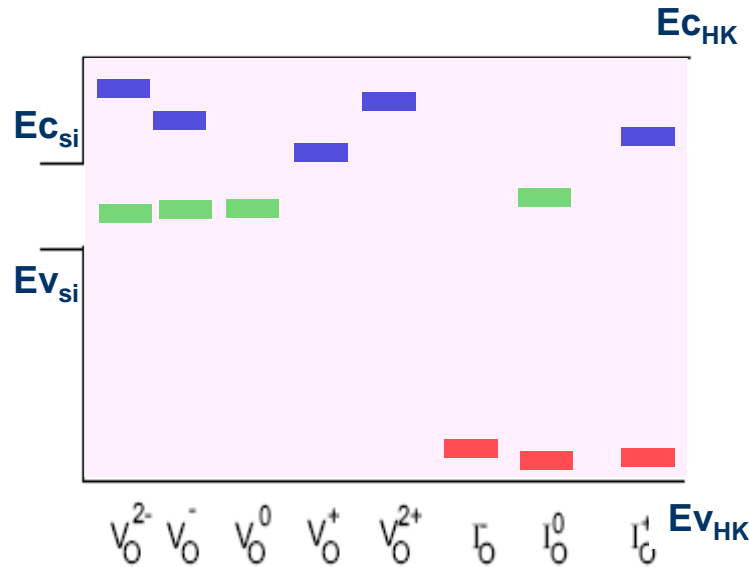
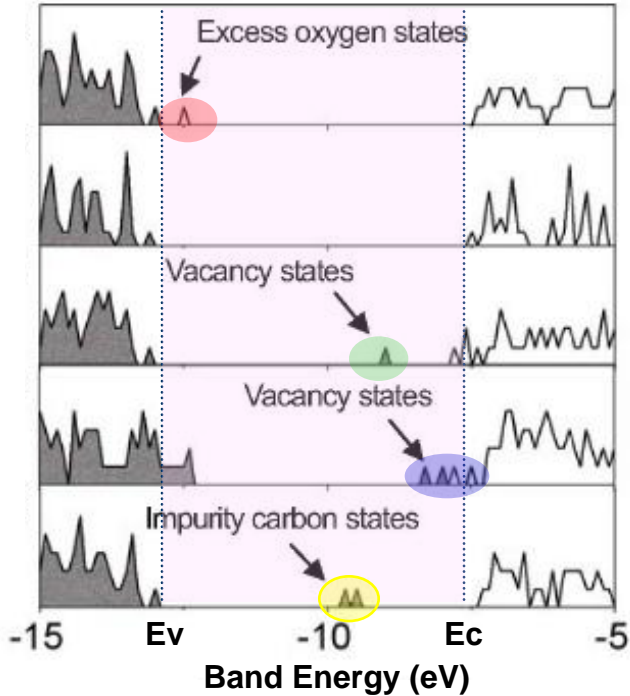


- Oxygen atoms have the tendency to diffuse into Si sub and MG.
- Formation Oxygen vacancy ( $V_o^+$ ) or Oxygen interstitial ( $I_o^-$ ) in hiK layer.
- Formation of SiOx IL (below hiK) and MOx IL layer (above hiK).
- Electron redistribution across IL's results in uncontrollable dipoles.

# Gap States Induced by Vo and Io

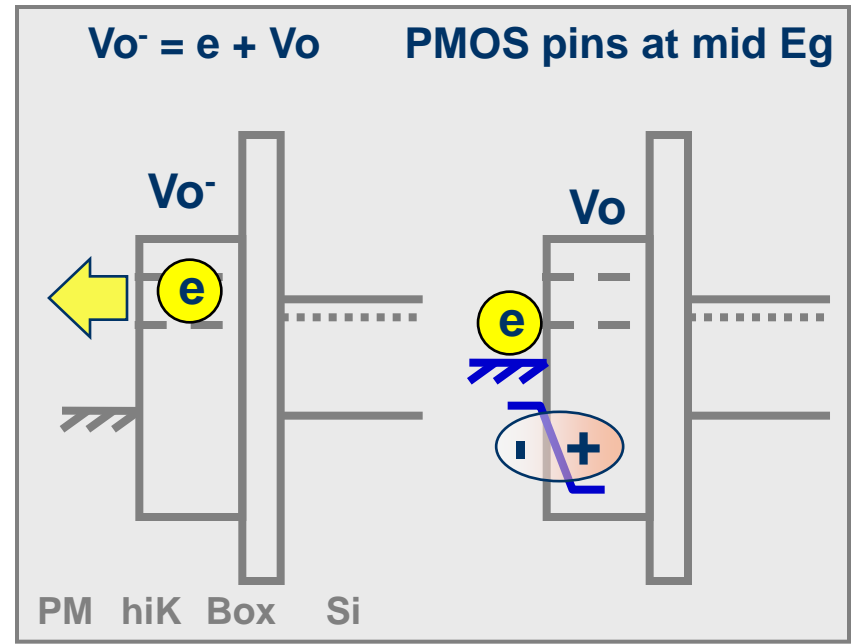
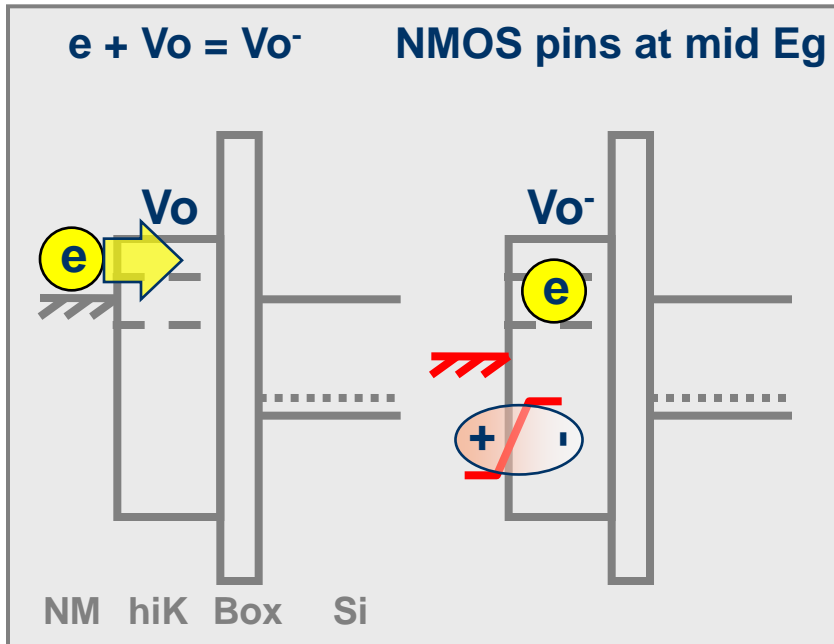
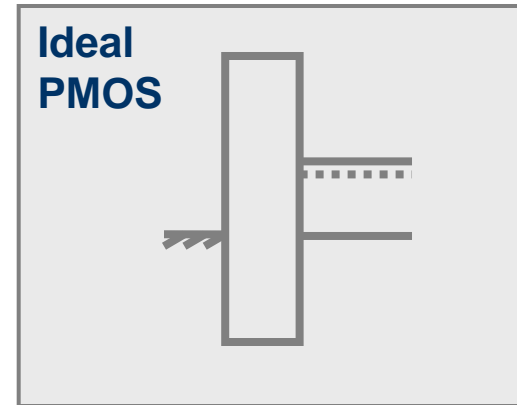
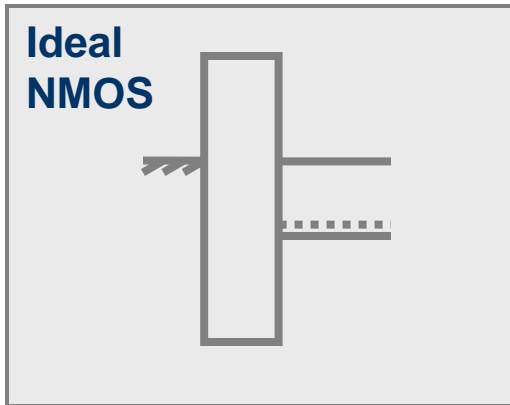


John Robertson Defect Energy levels in HfO<sub>2</sub>

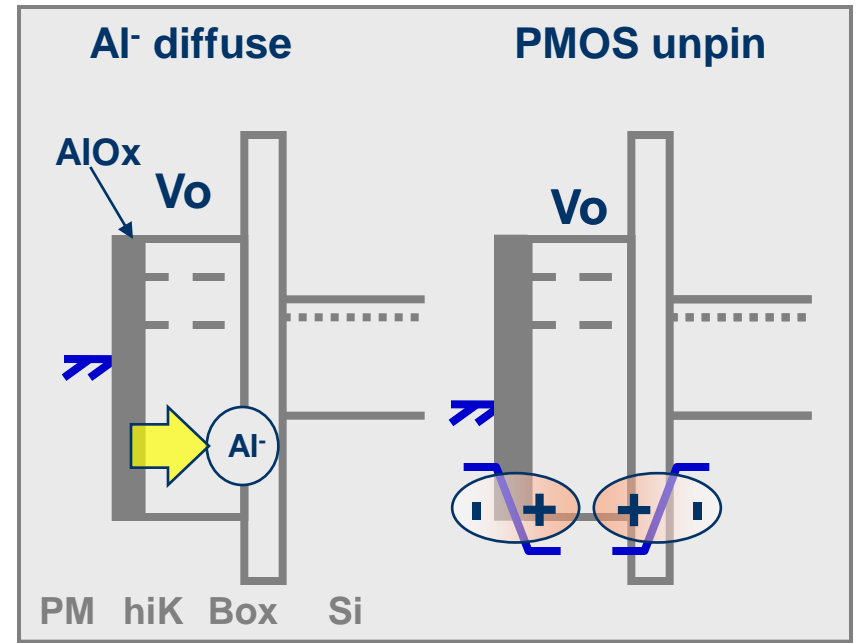
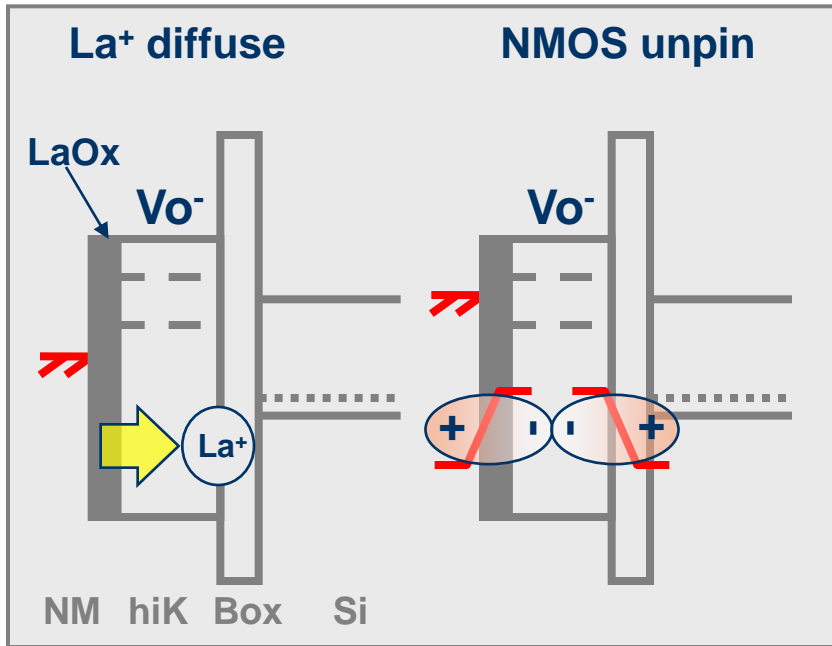
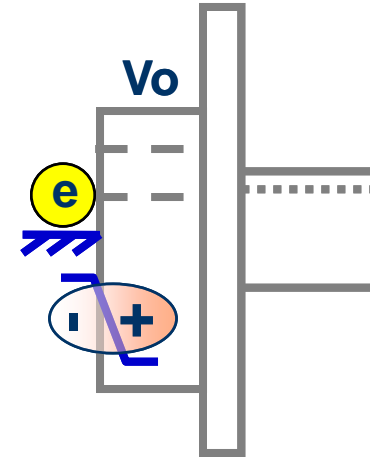
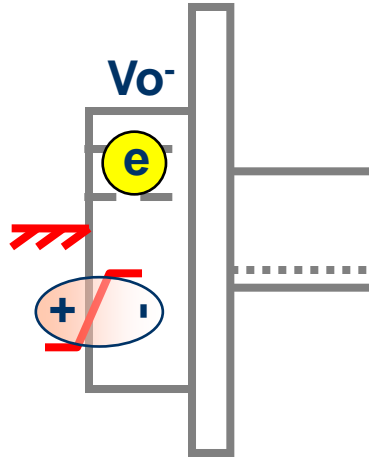


- Vo causes defect states near Ec edge, leads to electron leakage.
- Both Vo and Io reduce effective Bandgap of HfO<sub>2</sub>.
- Carbon atoms induce midgap states in HfO<sub>2</sub>, increase Jg.

# Fermi & $V_t$ Pinning by $V_o$ in $HfO_2$



# Resolving Fermi Pinning with Cap Layer

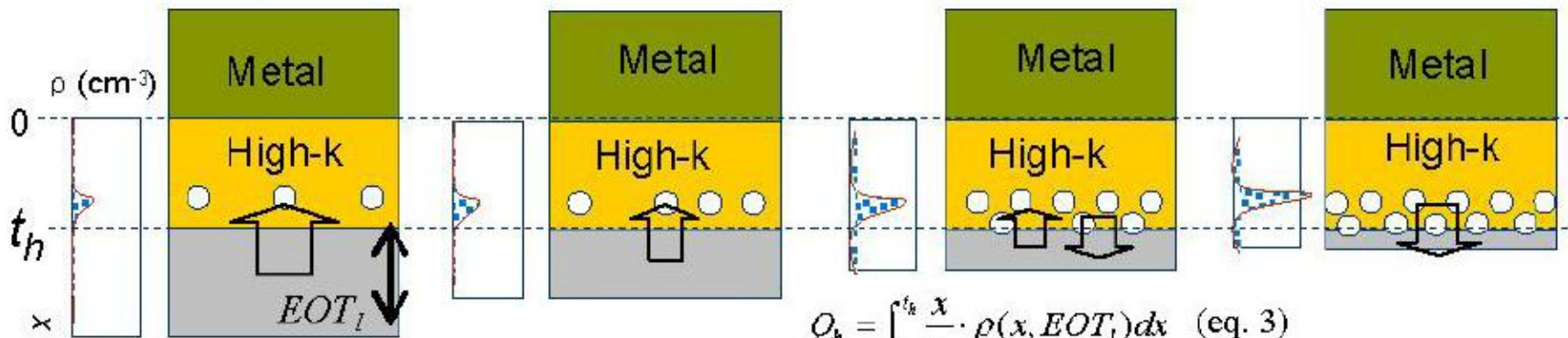
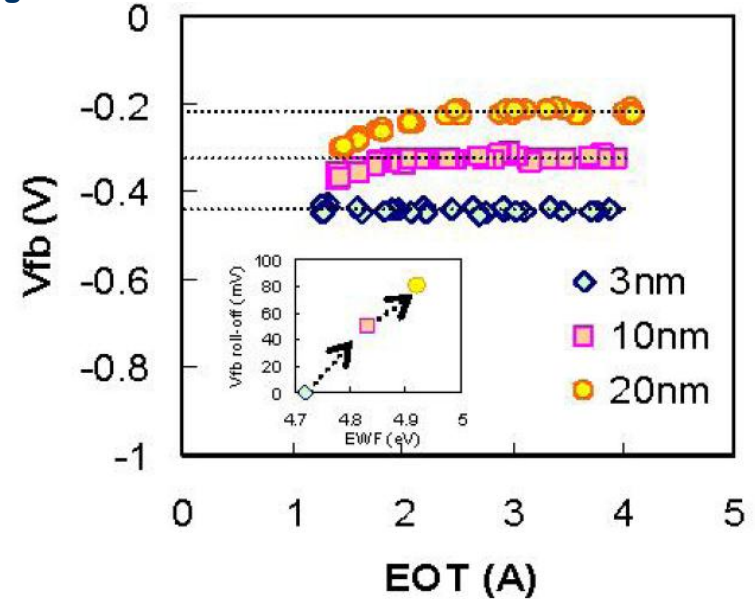
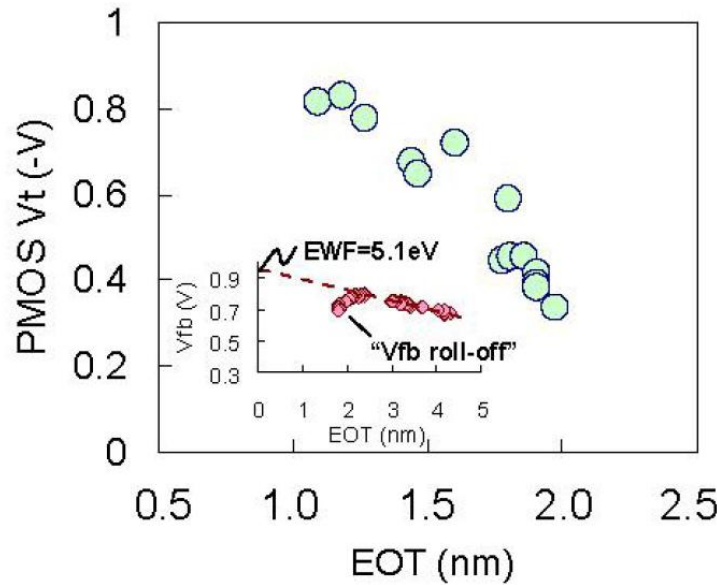


# Vo Induced Vt roll-off (Sematech)



Mechanism of  $V_m$  roll-off with High Work function Metal Gate and Low Temperature Oxygen Incorporation to Achieve PMOS Band Edge Work function

S. C. Song et al



$$Q_b = \int_0^{t_h} \frac{x}{t_h} \cdot \rho(x, EOT_1) dx \quad (\text{eq. 3})$$

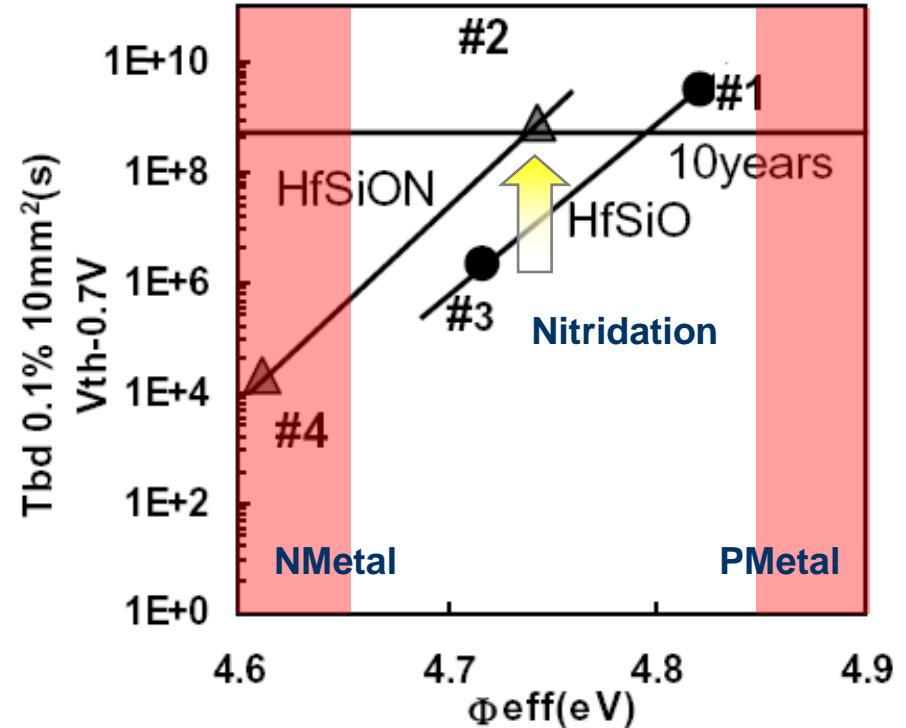
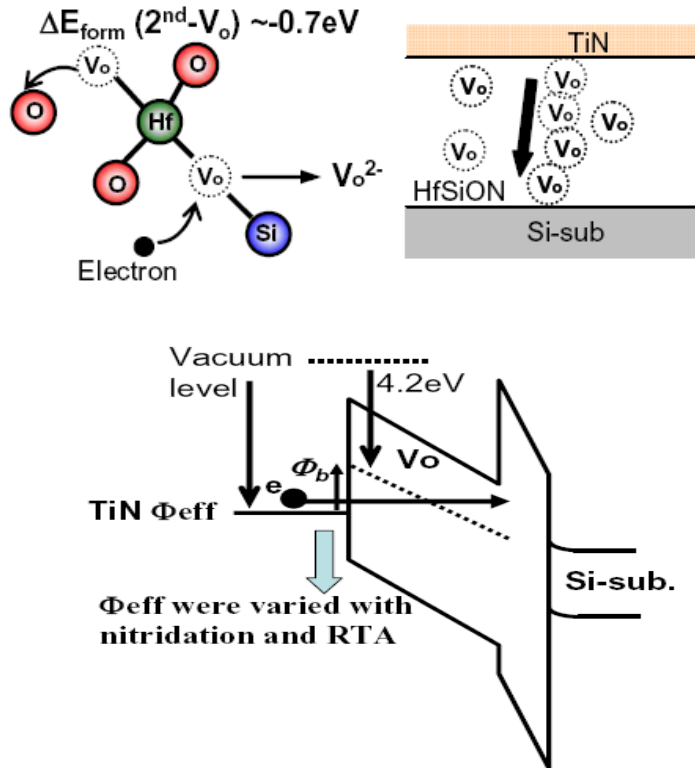
# Vo Induced Gate Leakage (Selete)



CATHODE ELECTRON INJECTION BREAKDOWN MODEL AND WORK FUNCTION  
DEPENDENT TDDDB LIFETIME FOR HIGH-K / METAL GATE STACK pMOSFETS

Motoyuki Sato et al

IEEE CFP08RPS-CDR 46<sup>th</sup> Annual International Reliability  
Physics Symposium, Phoenix, 2008



- $V_o$  chain reaction can be initiated by electron leakage current ( $J_{g_e}$ ).
- $J_{g_h}$  result in less  $V_o$  trap state generation than  $J_{g_e}$
- Nitridation passivates  $V_o$  and therefore improves  $T_{\text{bd}}$ .
- Low EWF metal will suffer more  $V_o$  generation within hiK, and thus lower  $T_{\text{bd}}$ .

