Fabrication and characterization of high-performance polymer thin-film transistors

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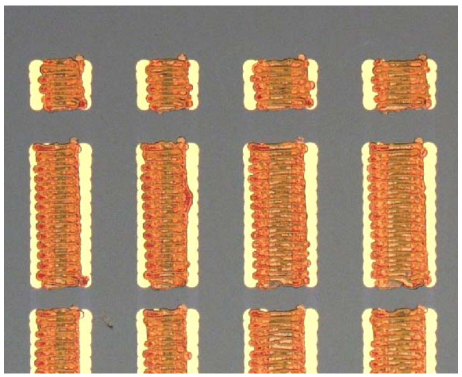

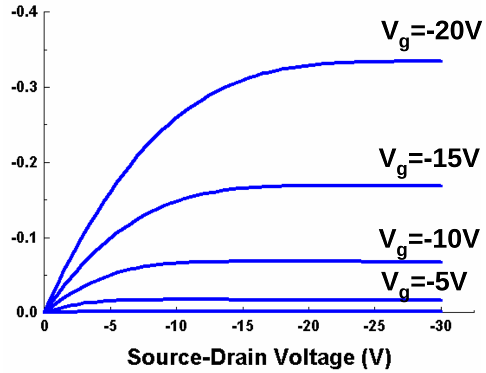

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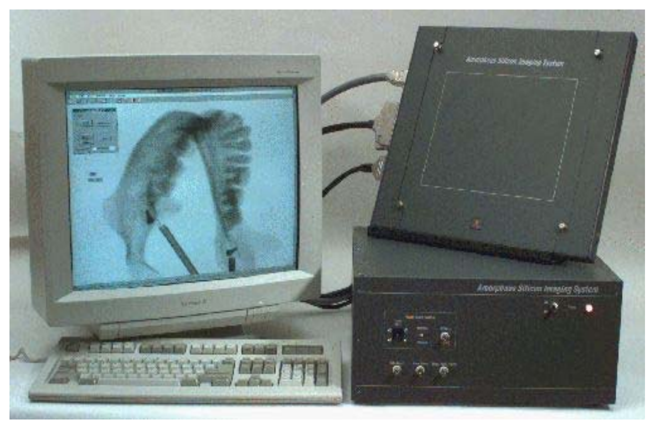
Large-area electronics

Source: Apple

Source: Gyricon Media



Source: dpiX

Low-T ⟶ Flexible substrates!

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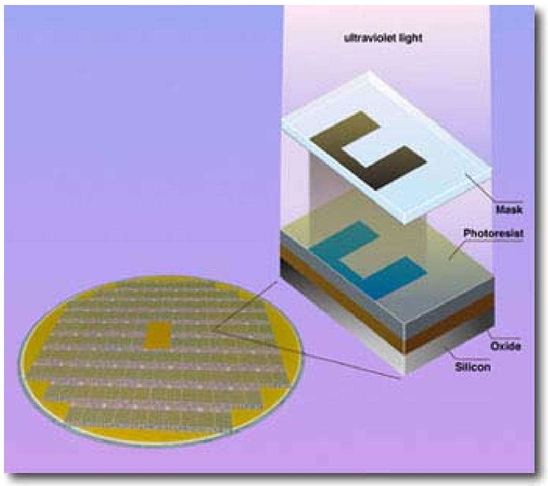
Alternatives to Photolithography

photolithography



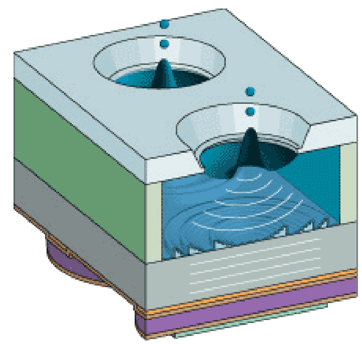
IBM

Screen Printing

web or sheet fed

simple

(Princeton, UCSC, UCLA)



AIP printhead - PARC

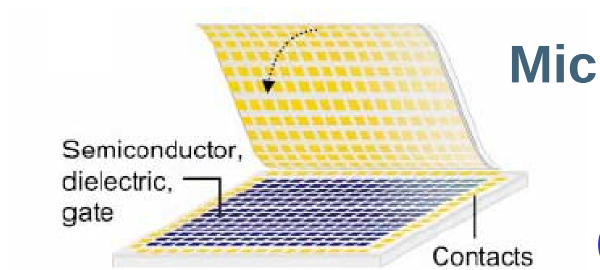
Jet-Printing

digital imaging

flexible substrates

direct-write of materials

(PARC, Plastic Logic)



Rogers, et. al. PNAS 2002

Microcontact Printing

small features

rapid patterning

(Harvard, Bell Labs, IBM)

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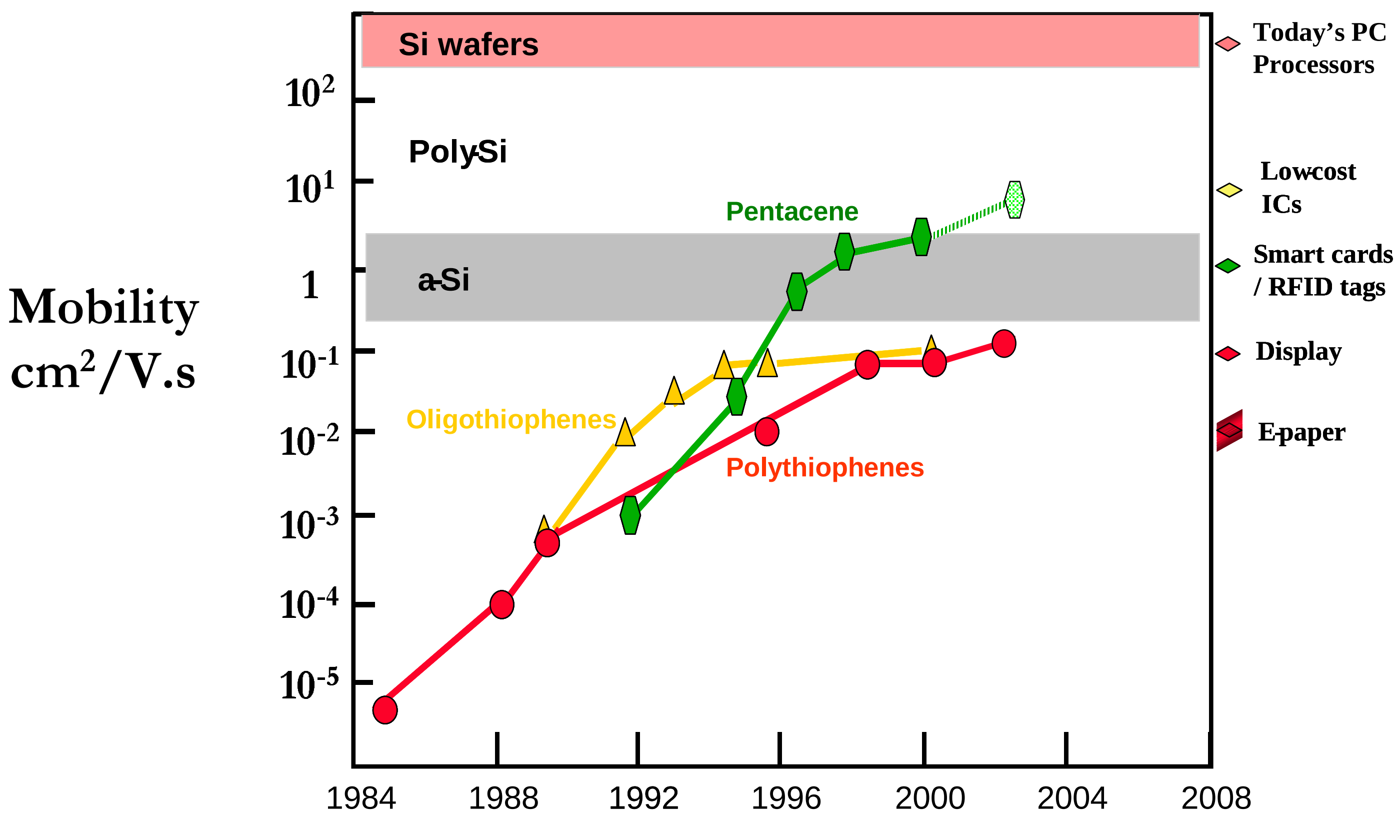
Challenges: materials compatibility, feature sizes, registration, process development

Outline

- Organic semiconductors
- Polymer thin-film transistors
- Patterning techniques
- Non-ideal behavior in polymer TFTs:
  - Contact resistance
  - Bias stress
  - Limits of polymer TFTs?

Organic semiconductors come in 2 “flavors”



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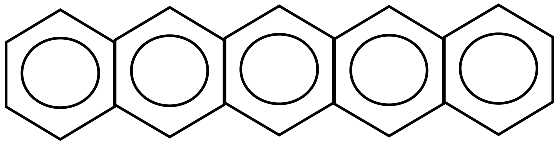
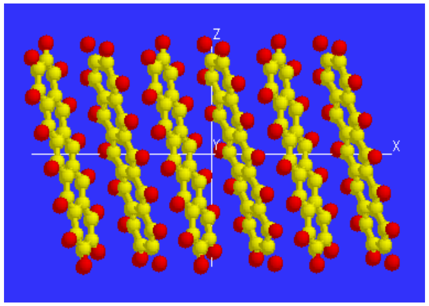
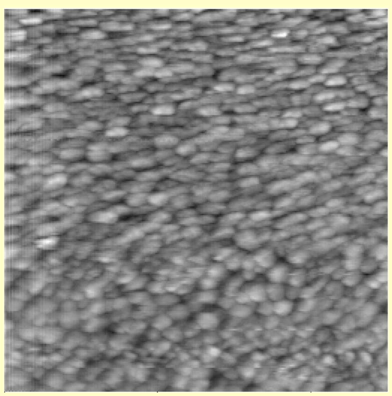
Pentacene is the best performing small molecule organic semiconductor



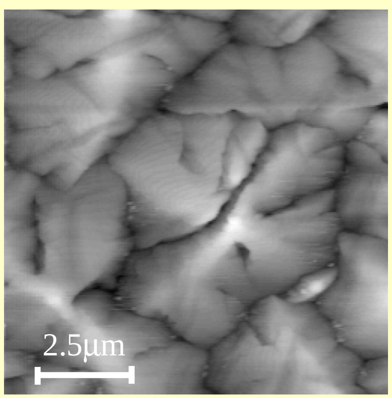


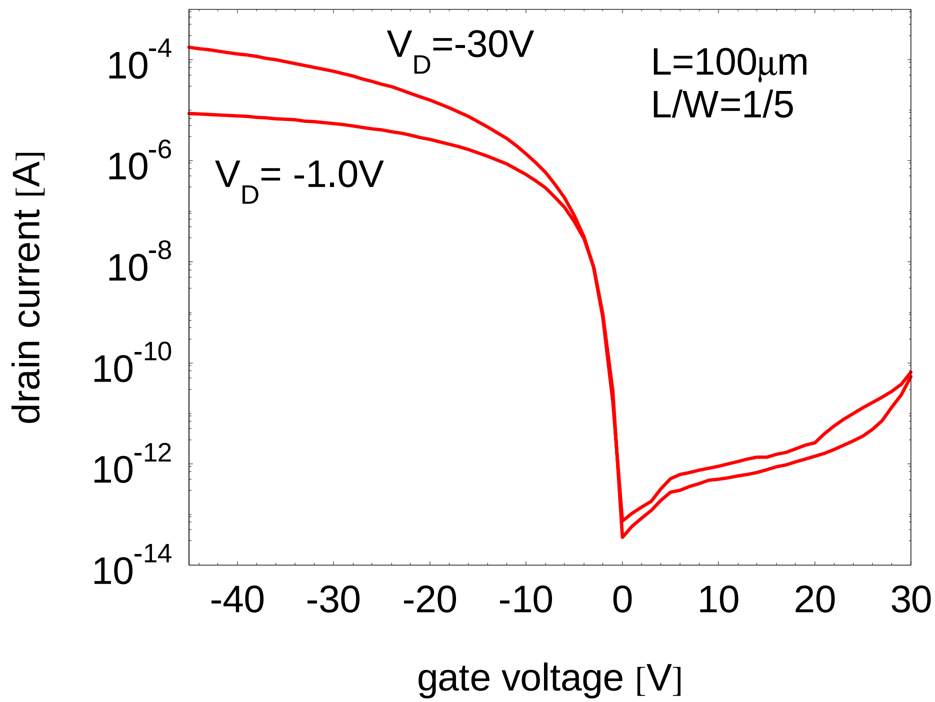
AFM

Low mobility



high mobility





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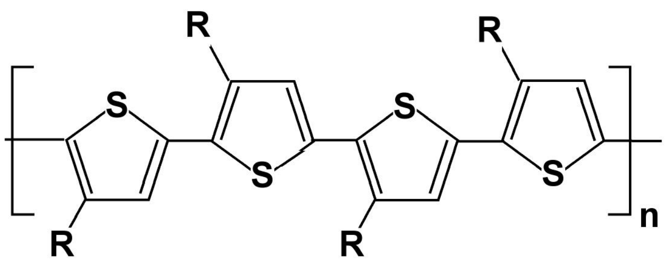
Polymeric Organic Semiconductors offer processing advantages

- deposited from solution
- amorphous or semicrystalline films
- good mechanical properties for flexible substrates

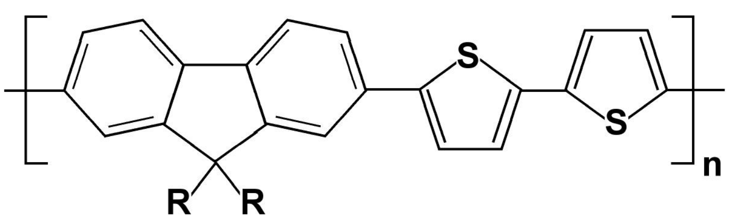
XPT: regio-regular poly(thiophene)



mobility ~ 10^{-2} to 10^{-1} $cm^2\ V^{-1}\ s^{-1}$

Xerox Research Centre Canada

F8T2: poly(9,9-dioctylfluorene-co-bithiophene)



mobility ~ 10^{-3} to 10^{-2} $cm^2\ V^{-1}\ s^{-1}$

Dow Chemical

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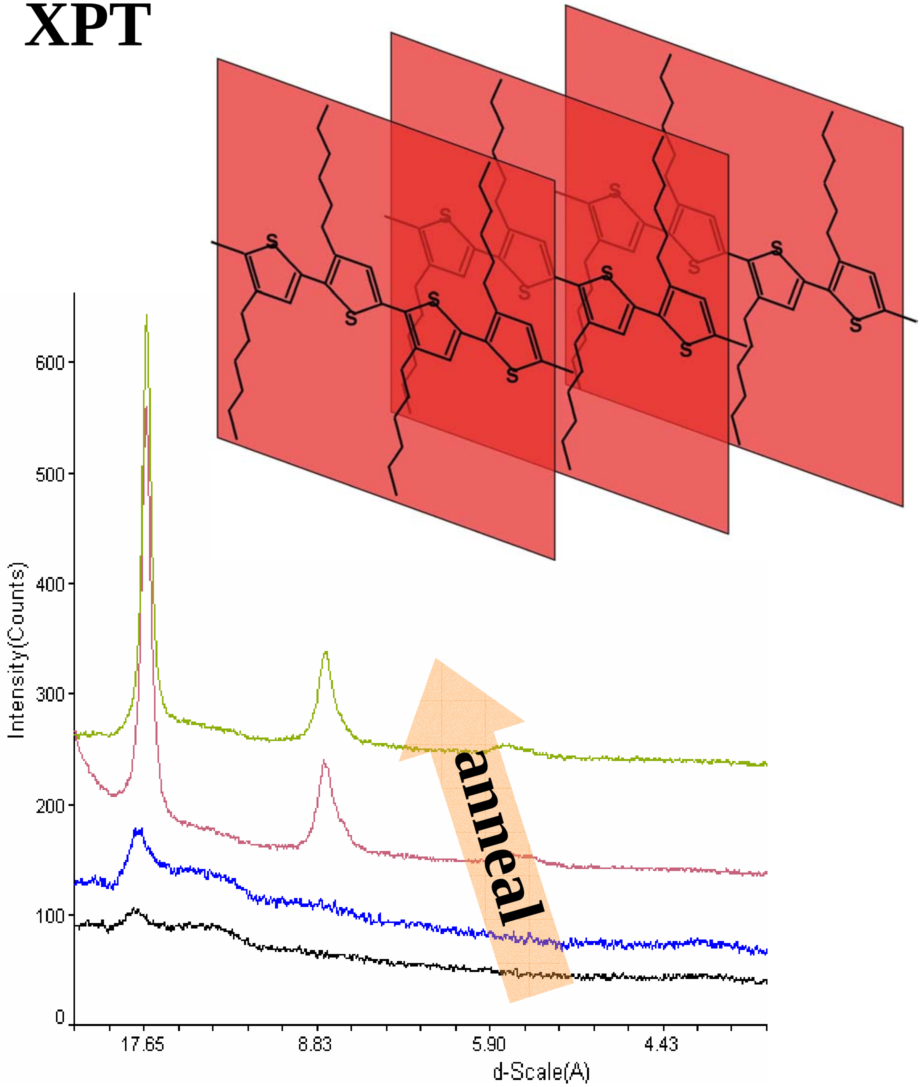
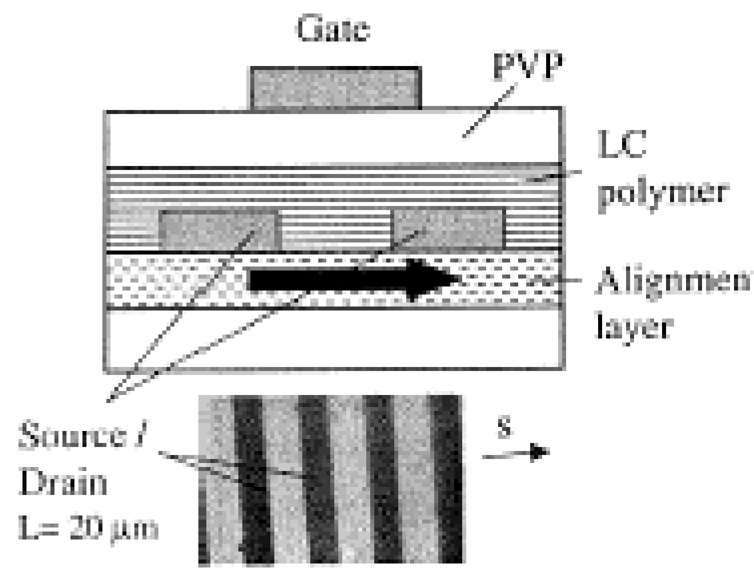
Carefully designed polymers form ordered films

XPT



F8T2



H. Sirringhaus et al., APL 77(3), 406 (2000)

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Outline

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- Patterning techniques
- Non-ideal behavior in polymer TFTs:
  - Device structure and contact resistance
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Thin-film transistor

What is important?

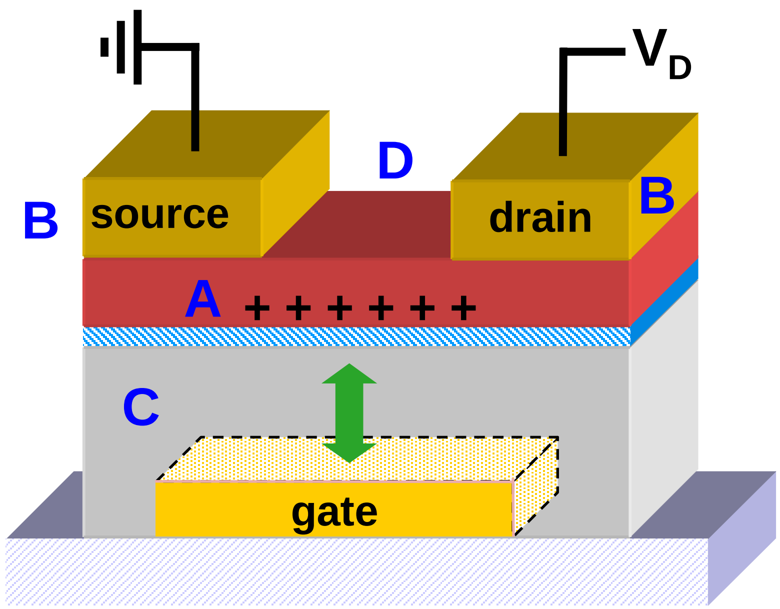
A. Conduction at the semiconductor-dielectric interface

B. Contacts - injection of holes, (and blocking of electrons)

C. Electronic stability

D. Ambient stability

E. Fabrication technology



$$I_D/V_D = (W/L)C_G \quad \mu_F \quad (V_G - V_T)$$

Conduction = geometry . mobility . voltage

(design material application)

Typical dimensions

Dielectric 100-500 nm

Semiconductor 20-50 nm

Channel “height” <1 nm

Channel length 2-100 μm

Channel width 10-500 μm

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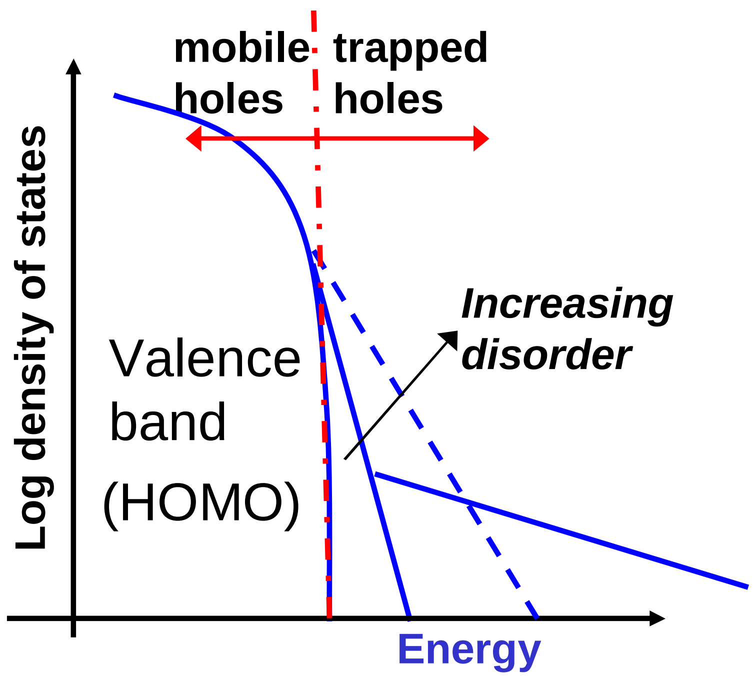
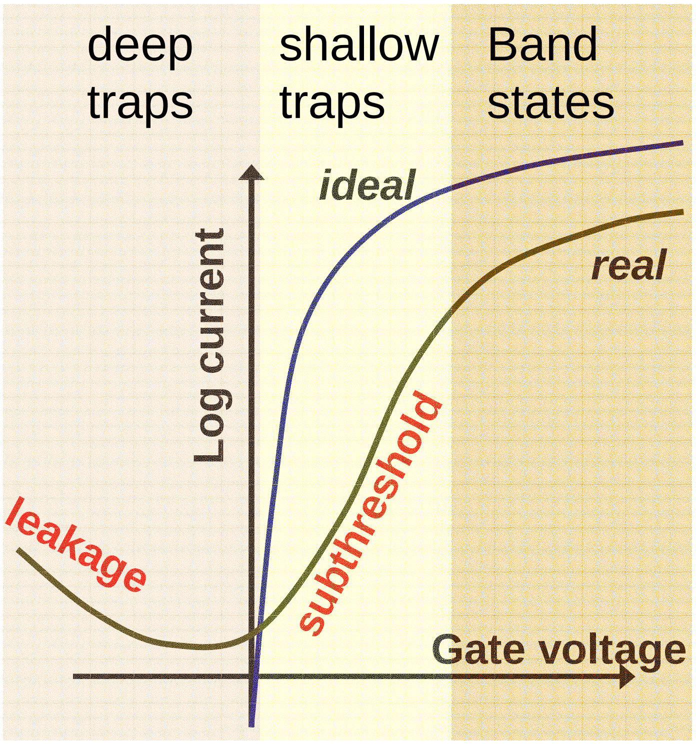
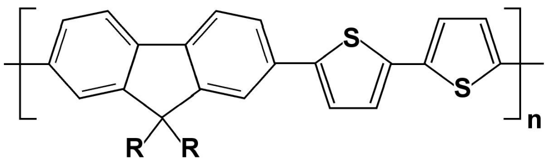
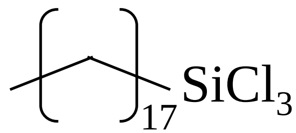
Disorder and TFT characteristics

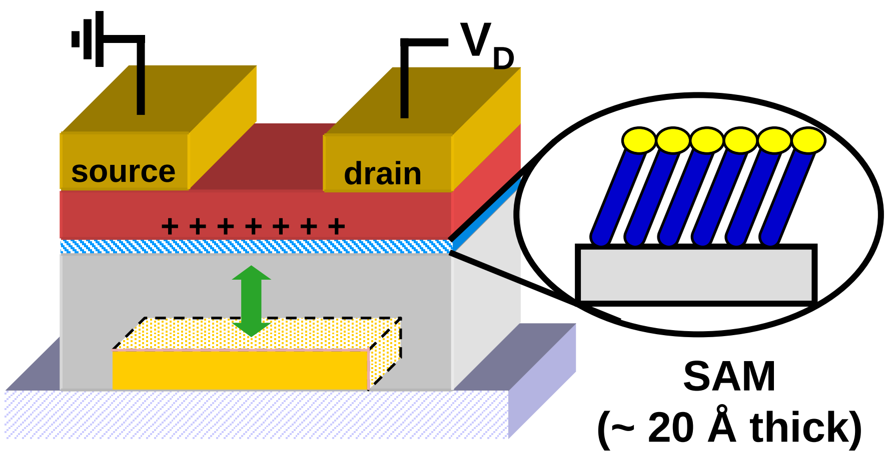


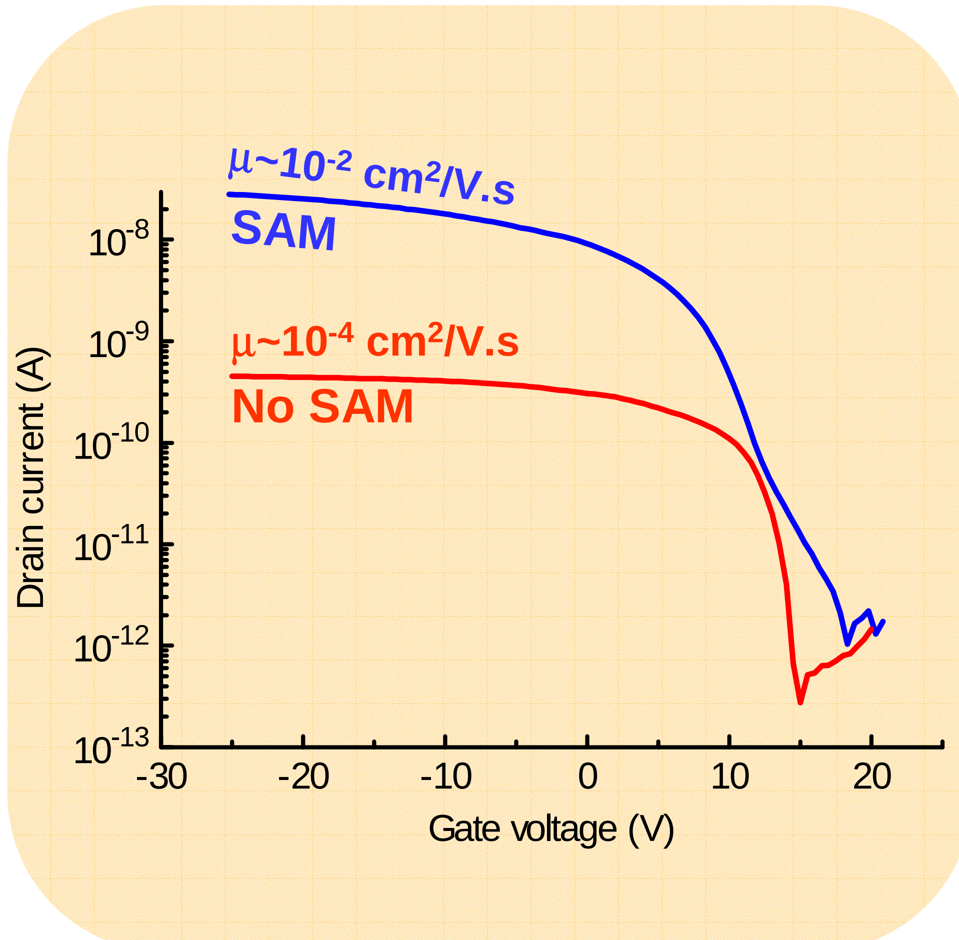


Chemically functionalized dielectric surface greatly enhances mobility



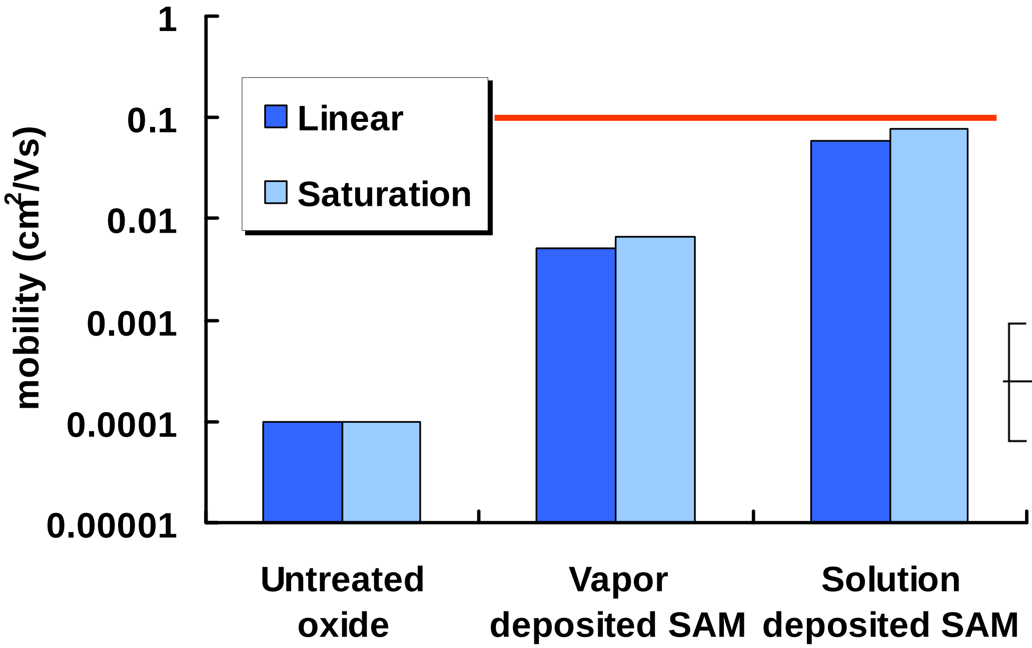


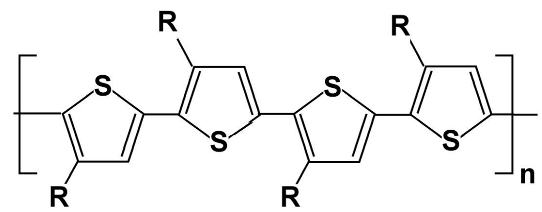


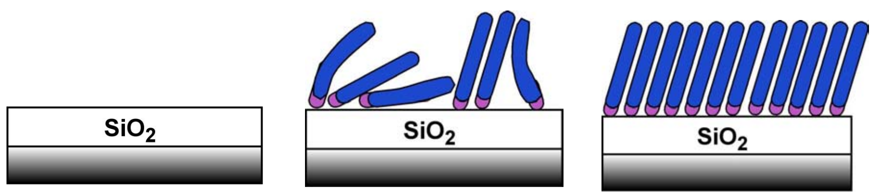


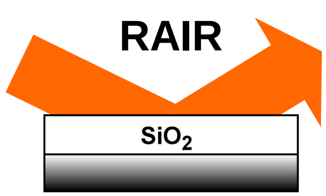
A. Salleo, M. L. Chabinyc, M. S. Yang, R. A. Street
APL 81(23), 4383 (2002)

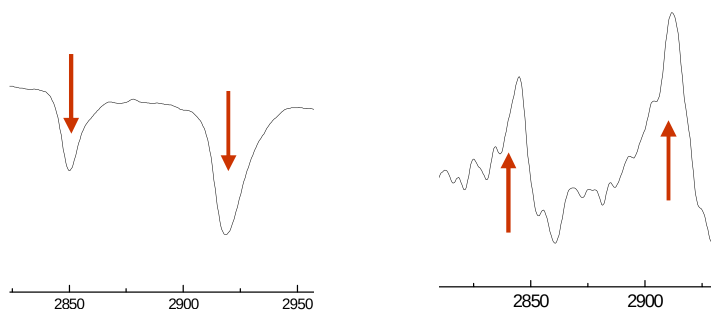
Mobility enhancement controlled by molecular ordering at the interface







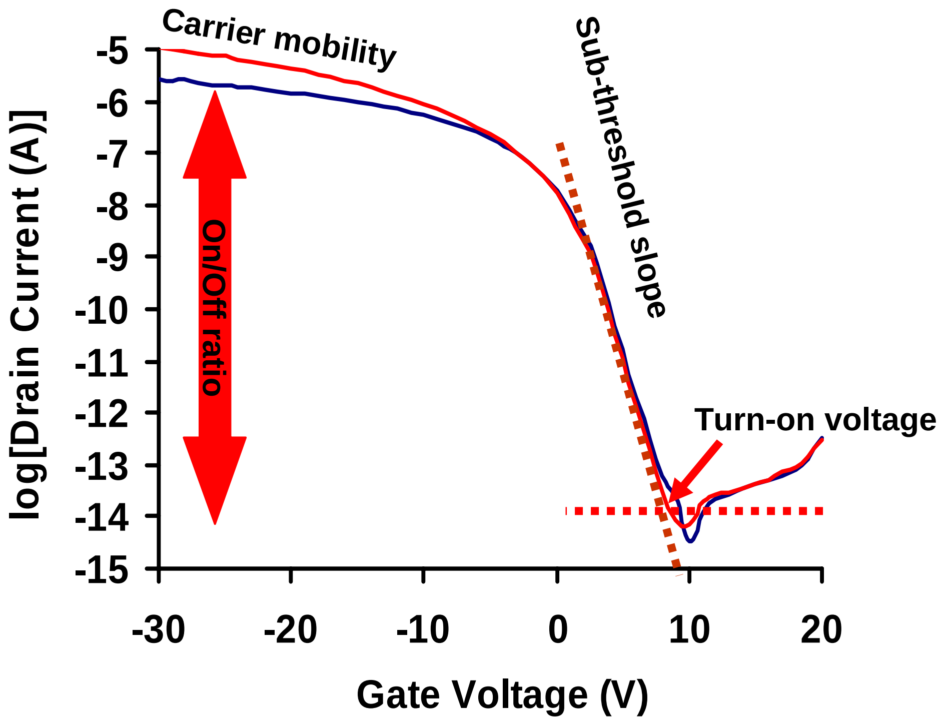


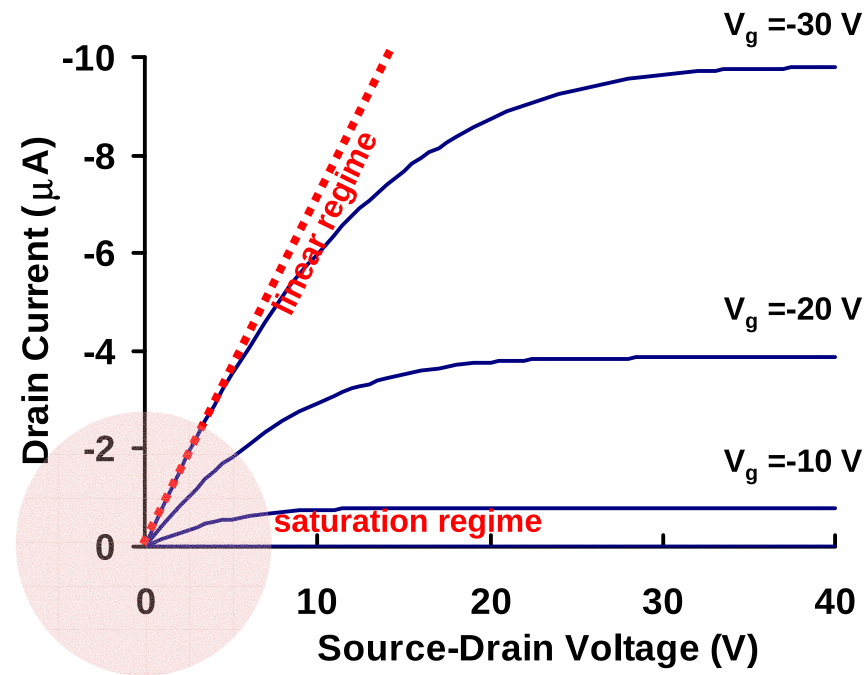


High-performance poly(thiophene) transistor

μ~0.1 $cm^2/V.s$

I_{on}/I_{off} up to 10^9





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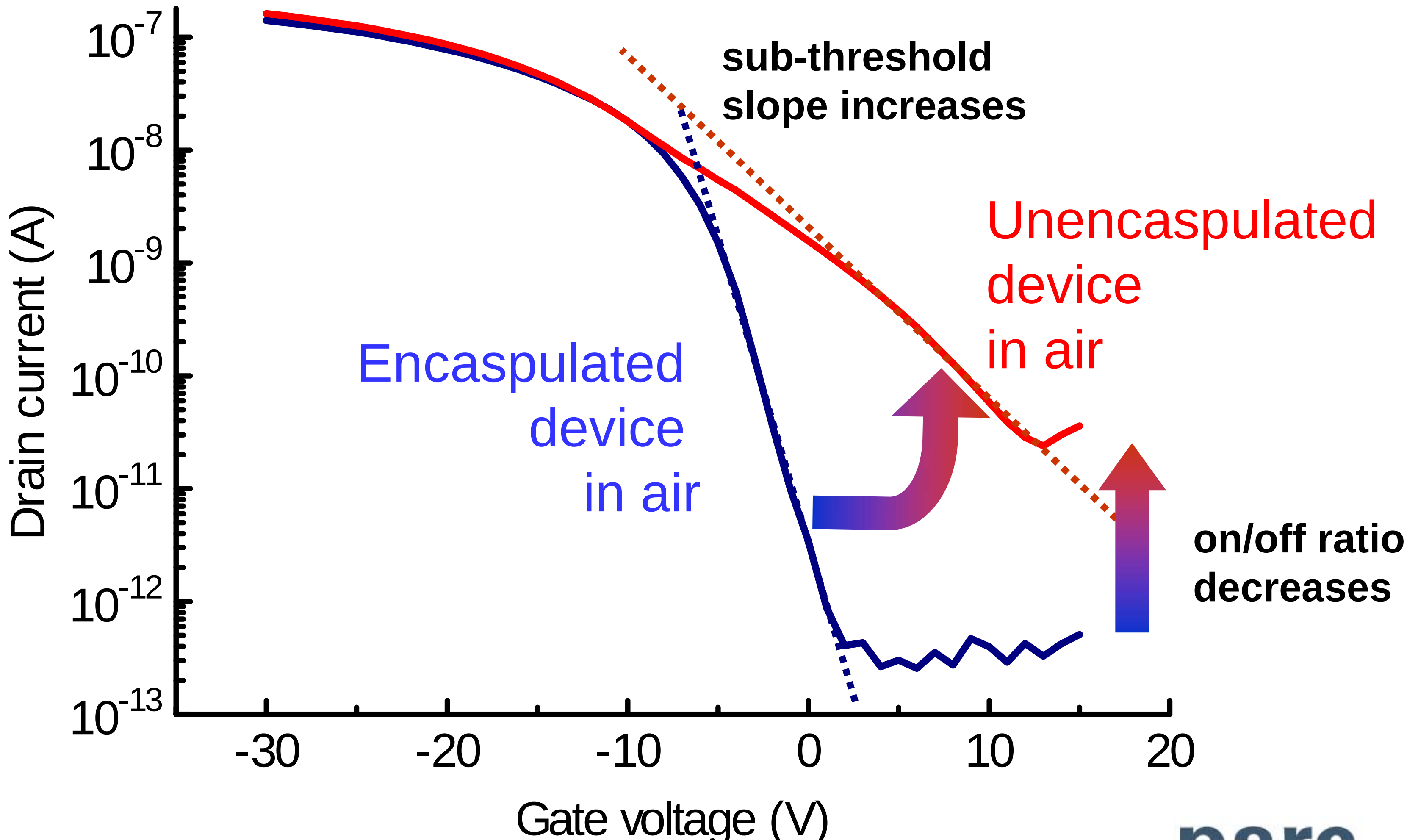
Environmental stability



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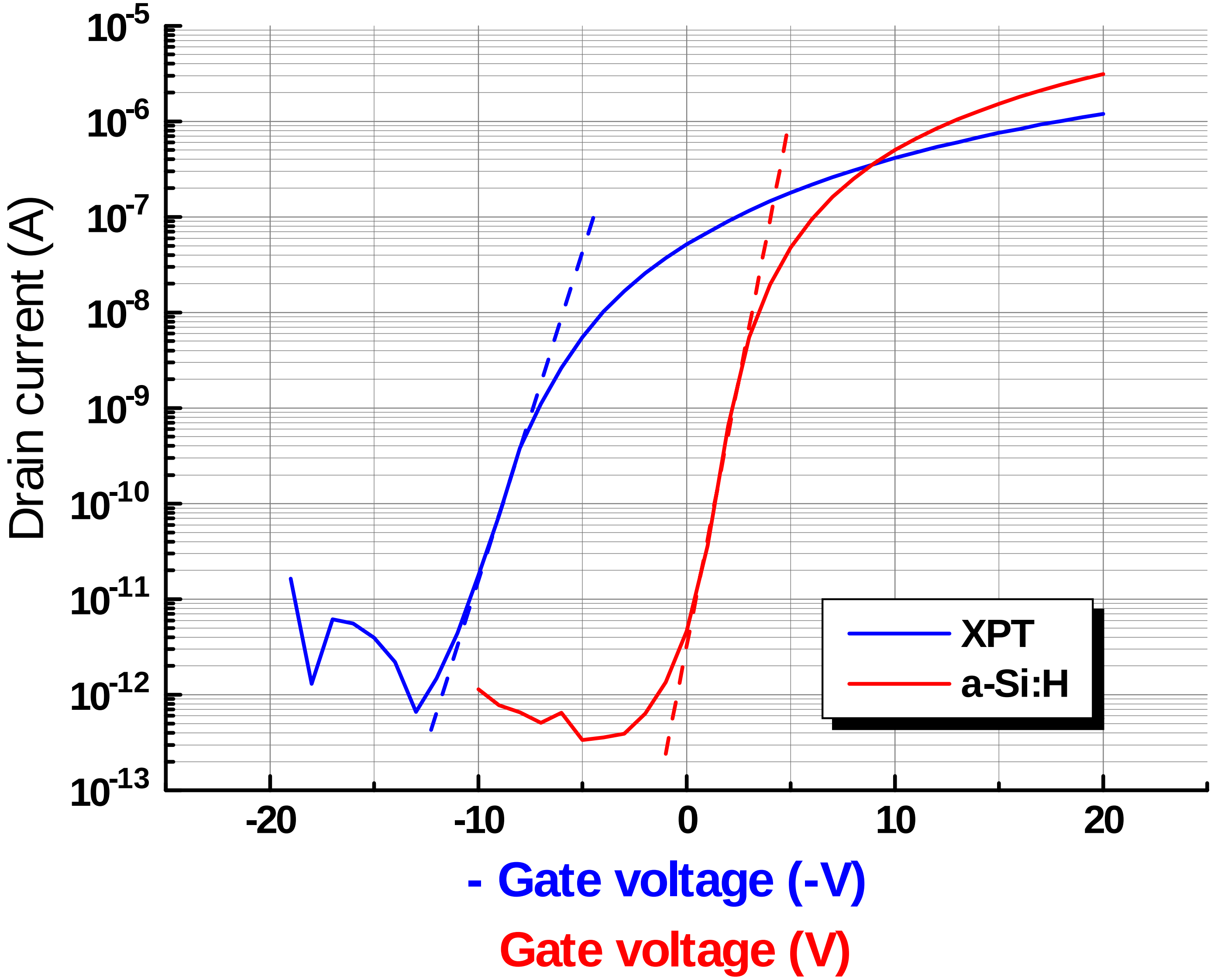
Where are we at this point?



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Outline

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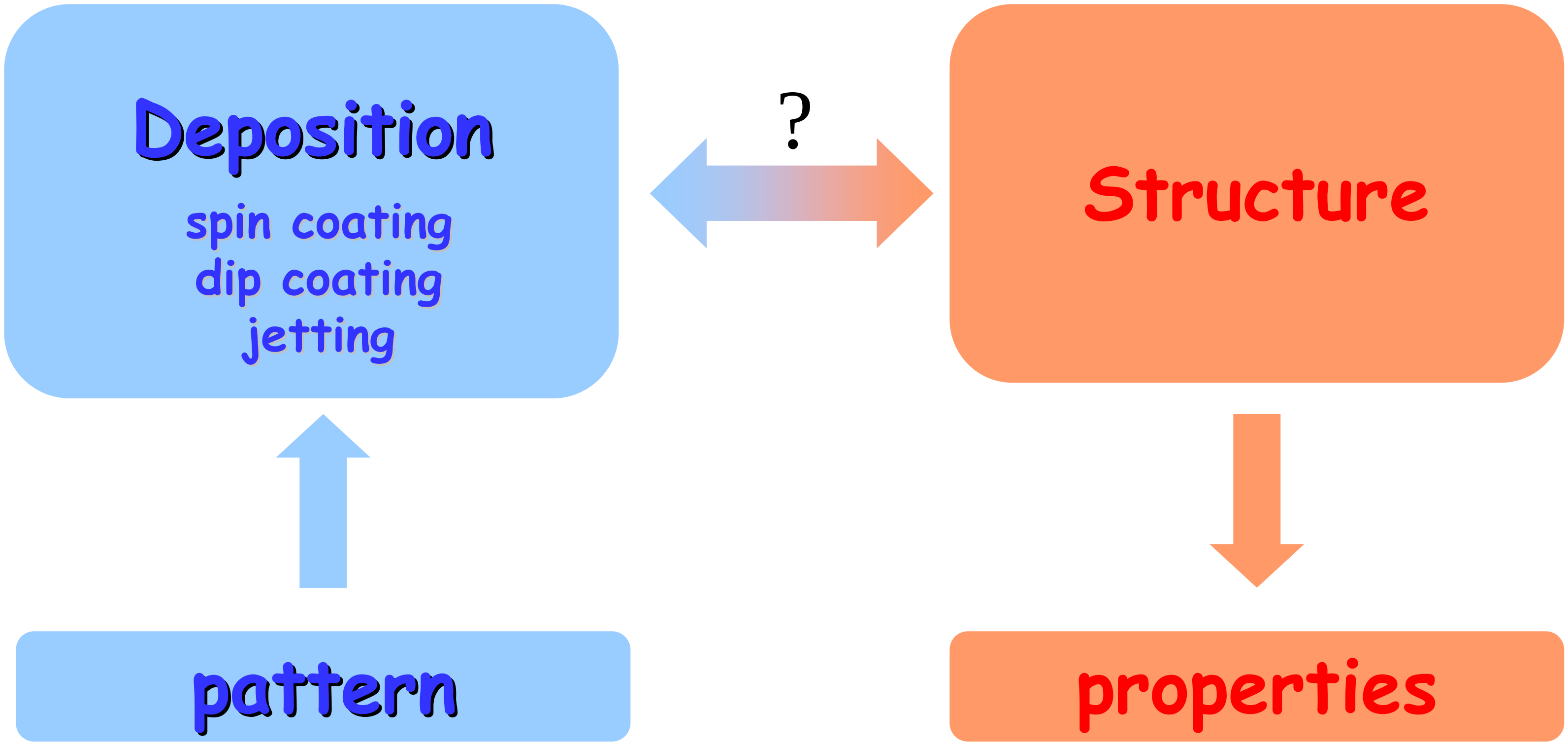
Patterning and properties



- Channel definition
- Device isolation
- Array design

- Carrier mobility
- On/Off ratio
- Stress

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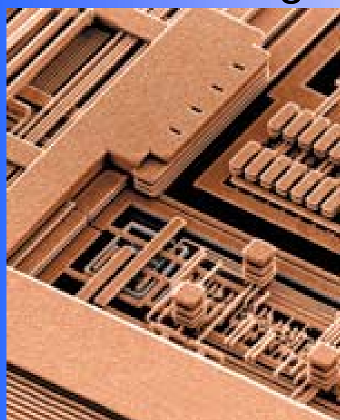
Patterning at “intermediate” scales enables use of non-conventional techniques

CMOS Processing

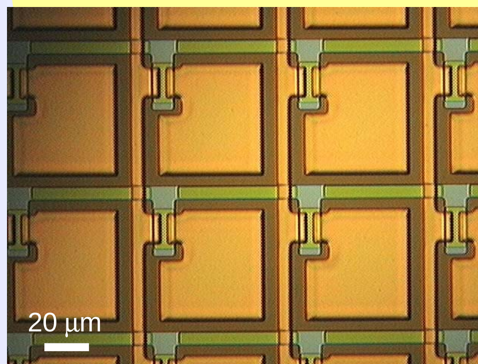


Source: IBM

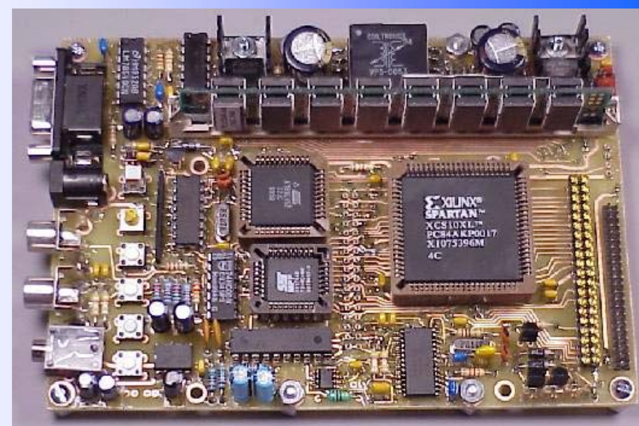
0.13-0.15 µm features

Target

5-20 µm features



Printed Circuit Board



100-500 µm features

Increasing feature size

Increasing cost

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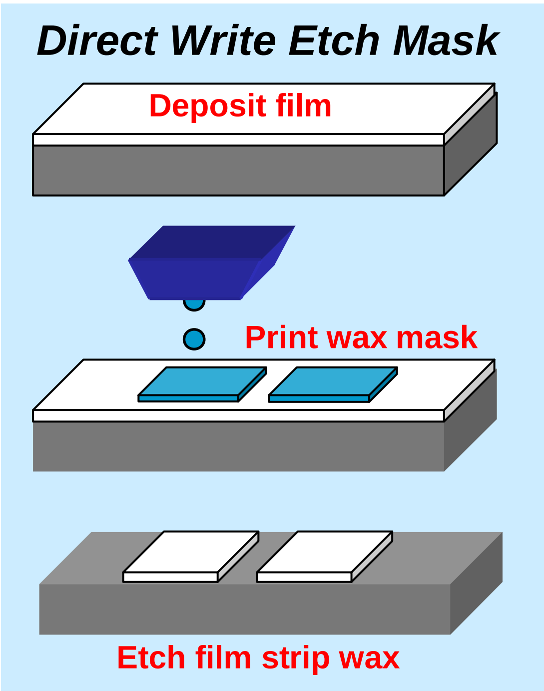
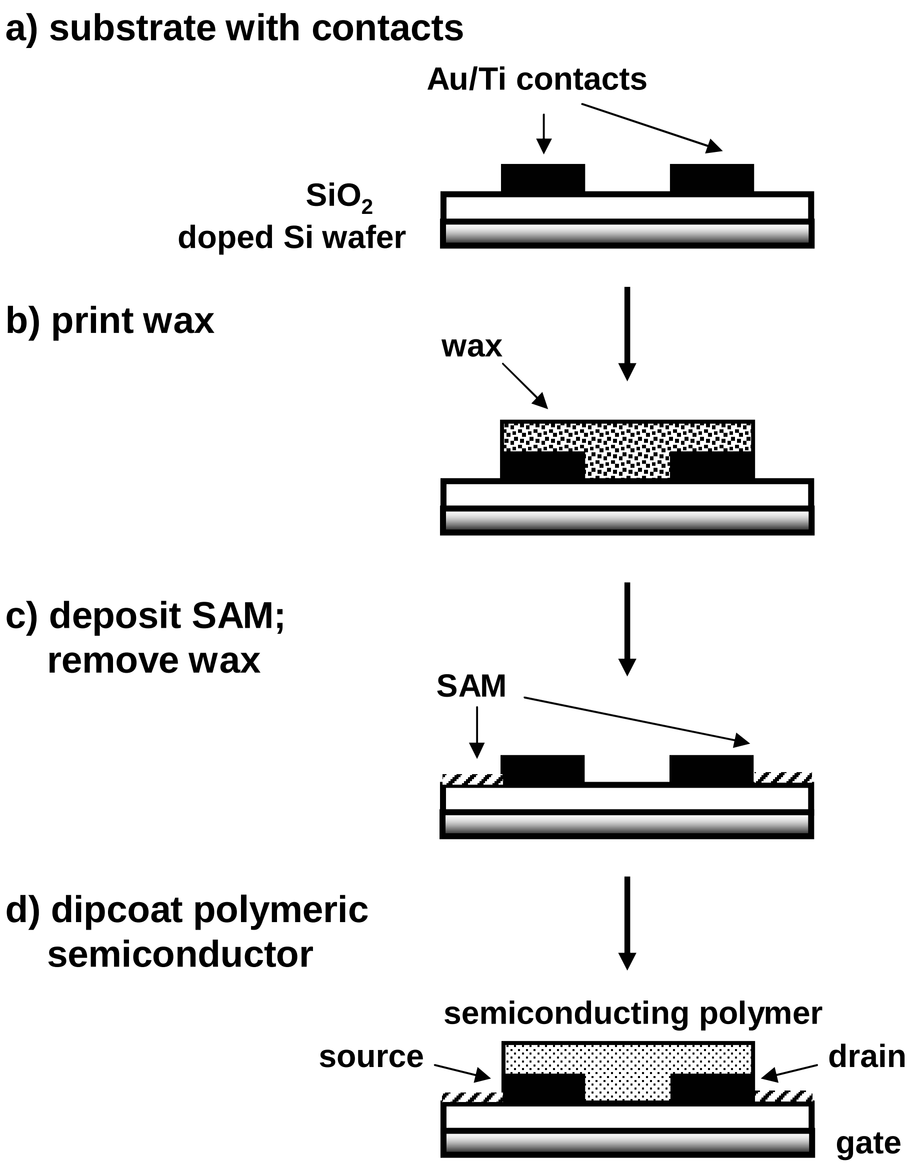
Ink-jet printing of wax is used to define the device structure

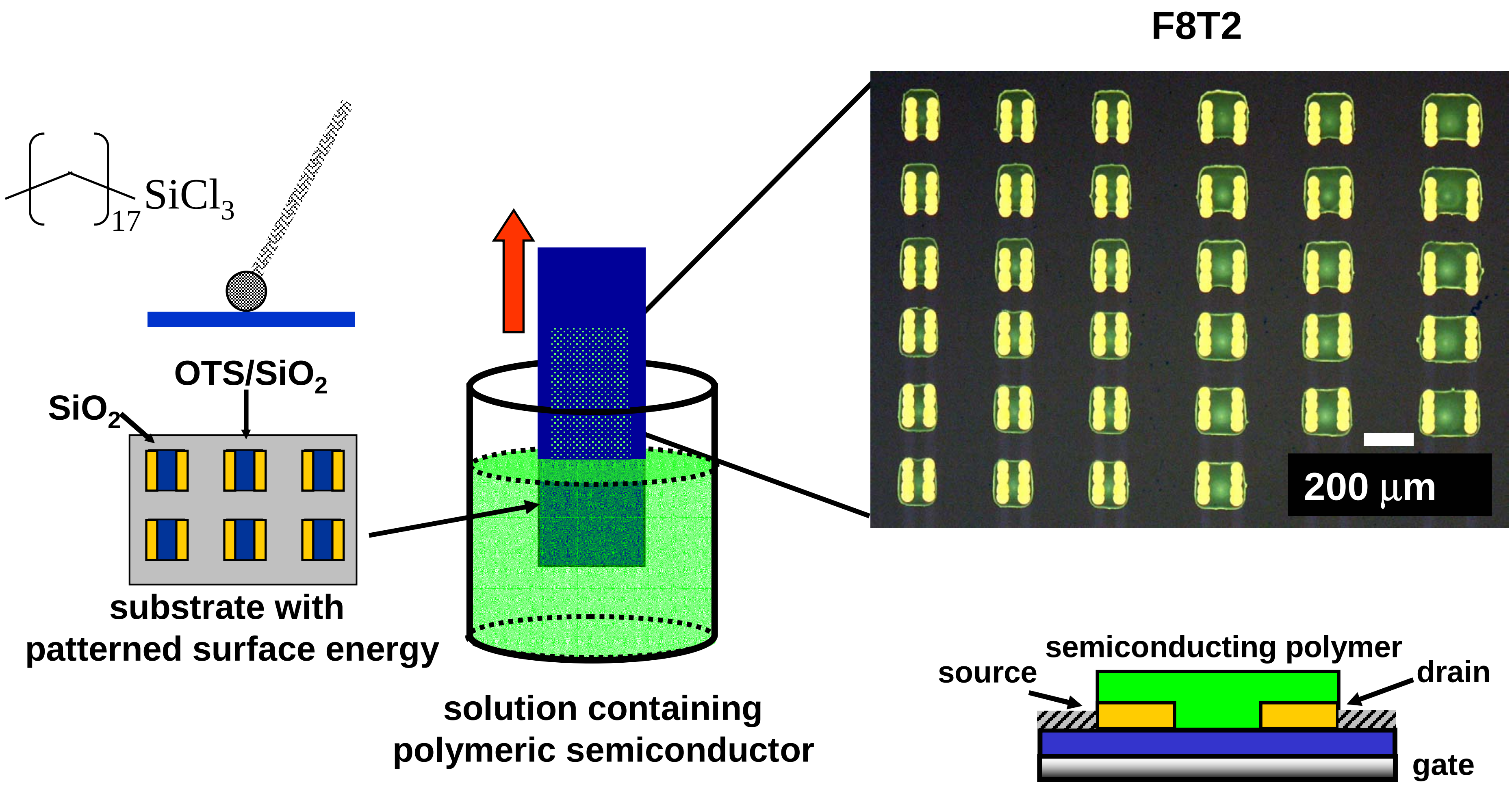


Layer registration



TFTs are completed by taking advantage of patterned dewetting

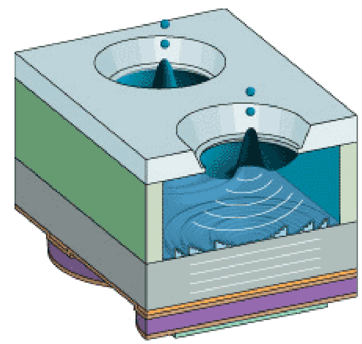
M. L. Chabinyc, W. S. Wong, A. Salleo, K. E. Paul, R. A. Street
APL 81(23), 4383 (2002)



Jet-printed Organic Semiconductors

- ***Additive process***
- ***Digital mask***
- ***Alignment better than 5 microns***
- ***Variety of substrates, dielectrics, surface treatments possible***
- ***Top or bottom contacts possible***

Direct deposition of active material



Acoustic inkjet printing (AIP)

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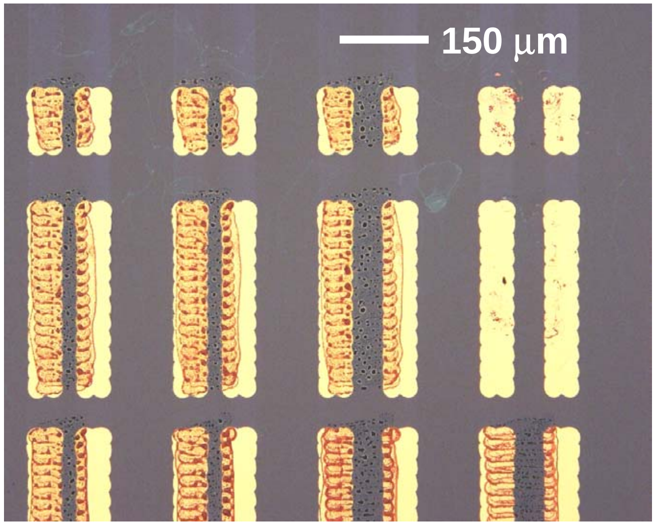
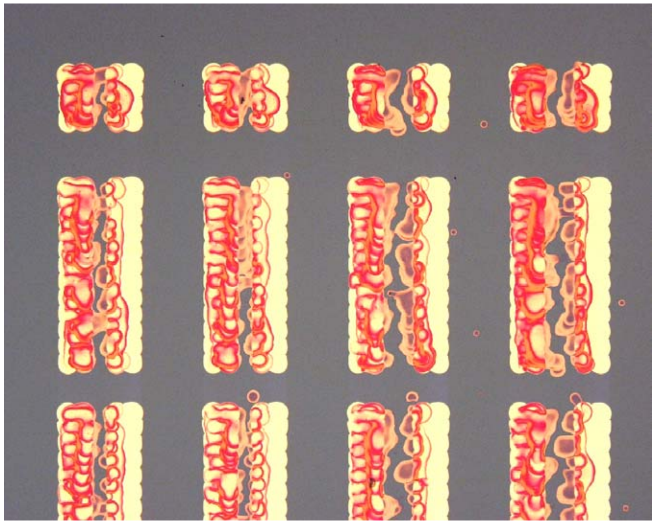
Ink-jet printing requires optimization

Semiconductor not dissolved



Semiconductor dewetting



Optimize

- ***Temperature of solution and substrate***
- ***Concentration of solution***
- ***Drop-to-drop overlap***
- ***Print speed***

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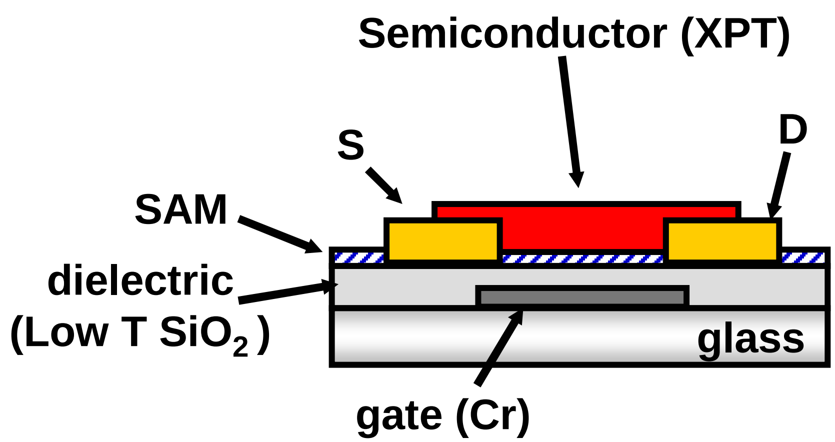
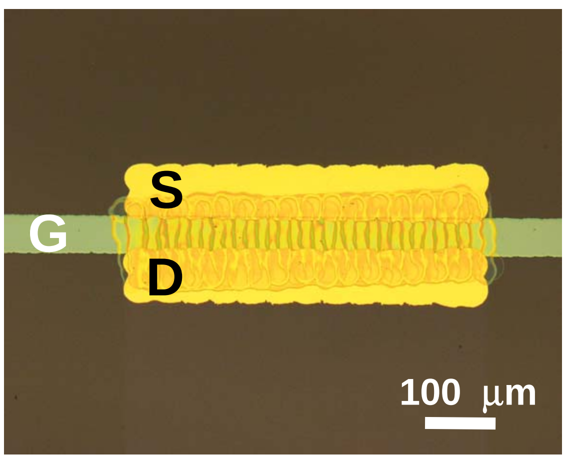
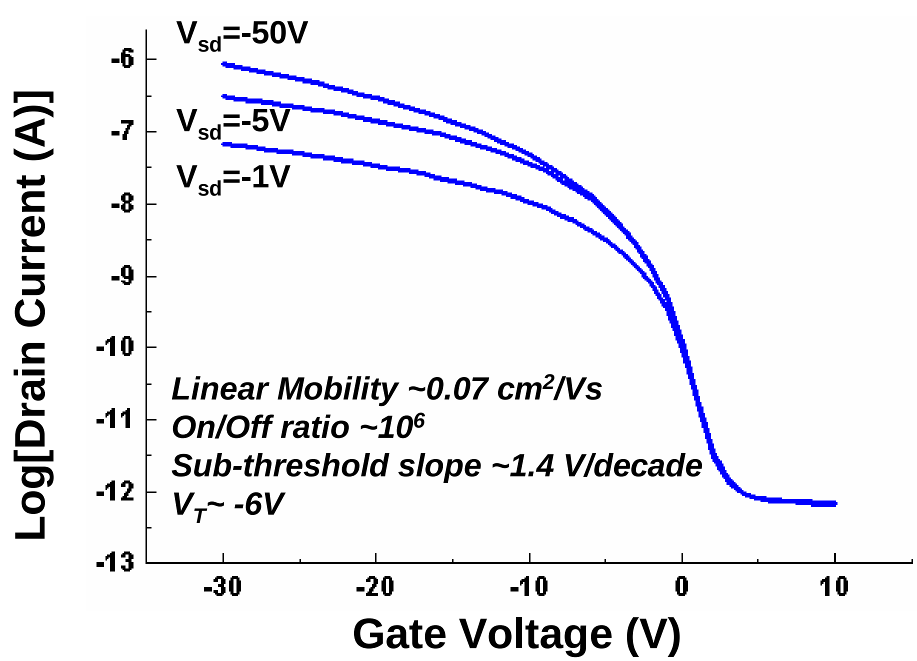
All print-patterned TFT







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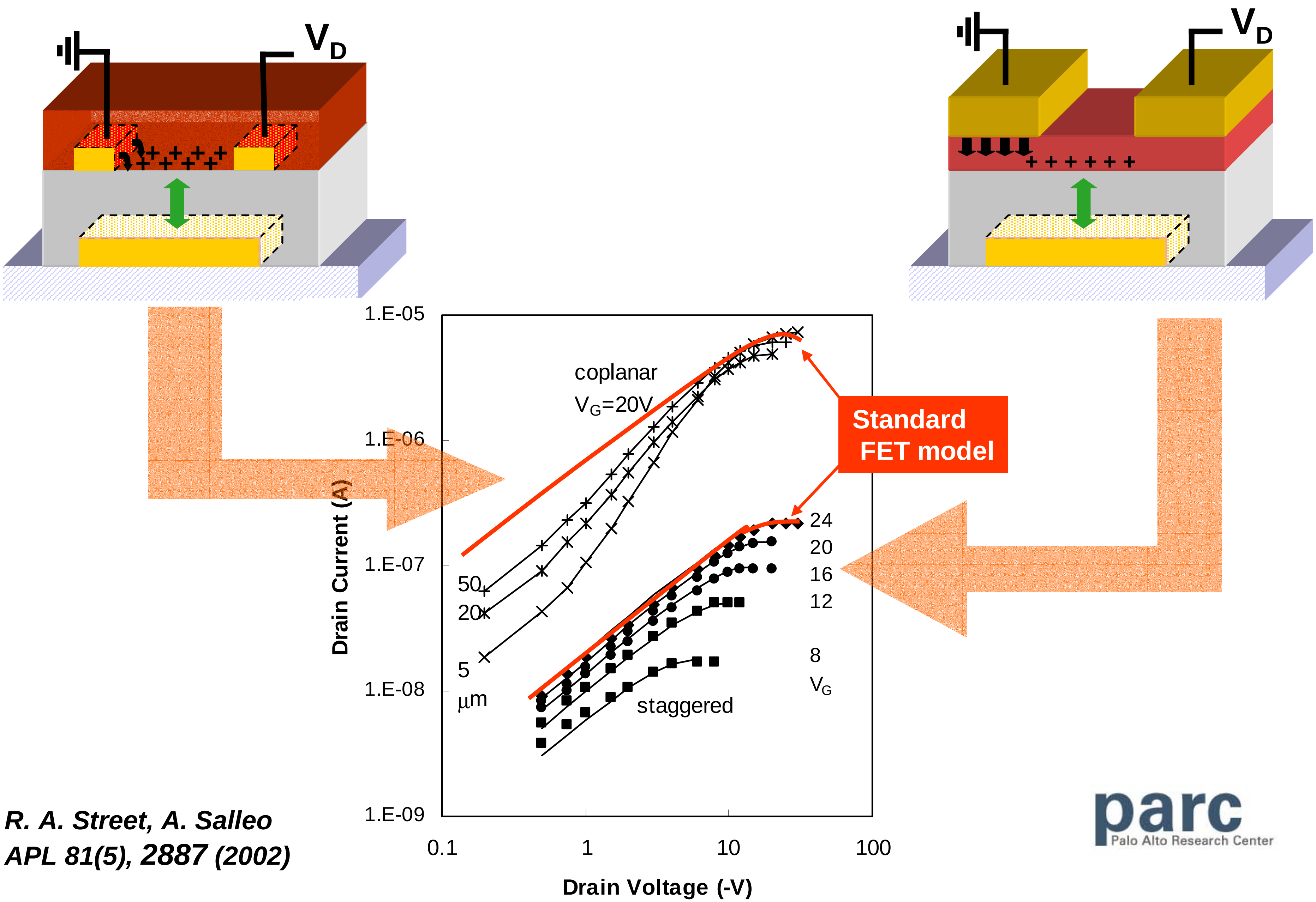
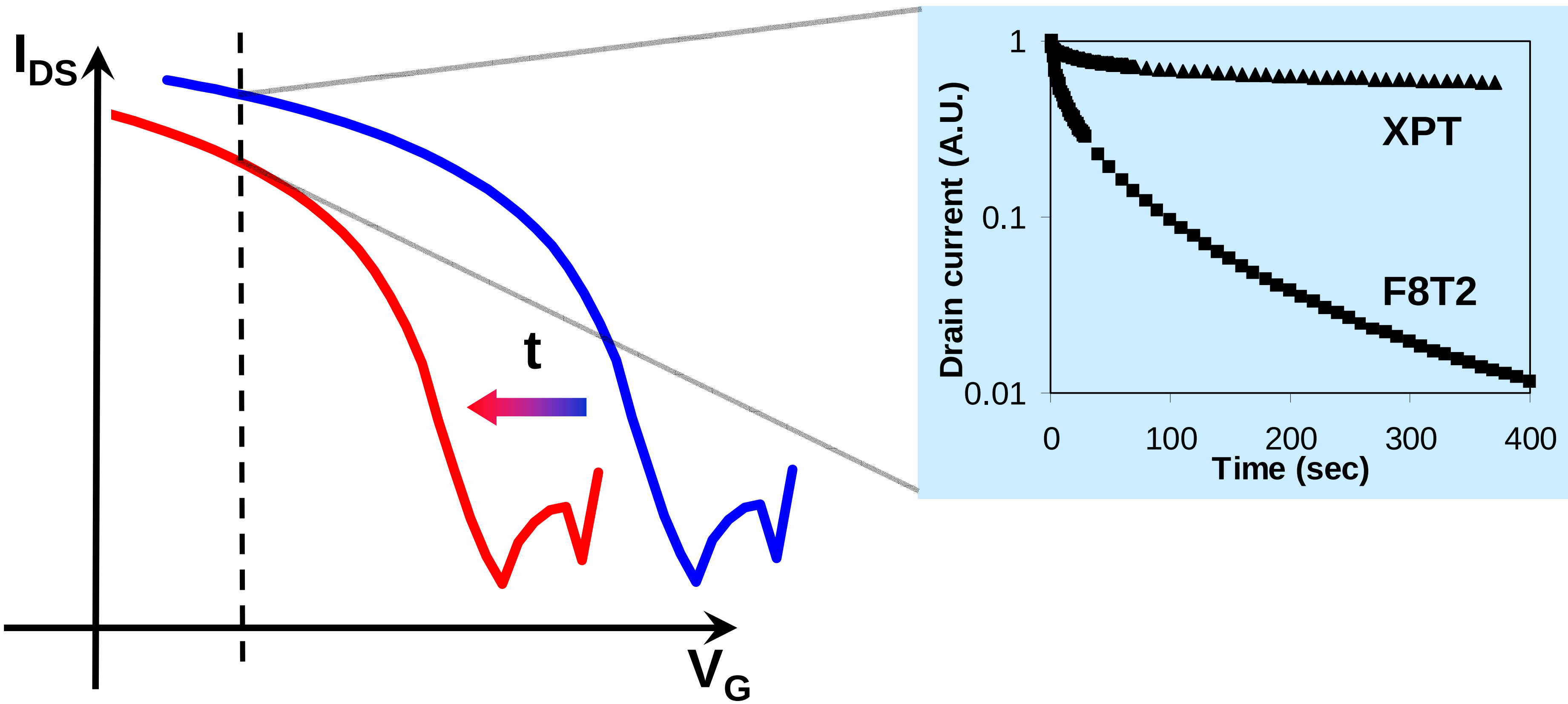
Staggered TFT performs better than coplanar TFT



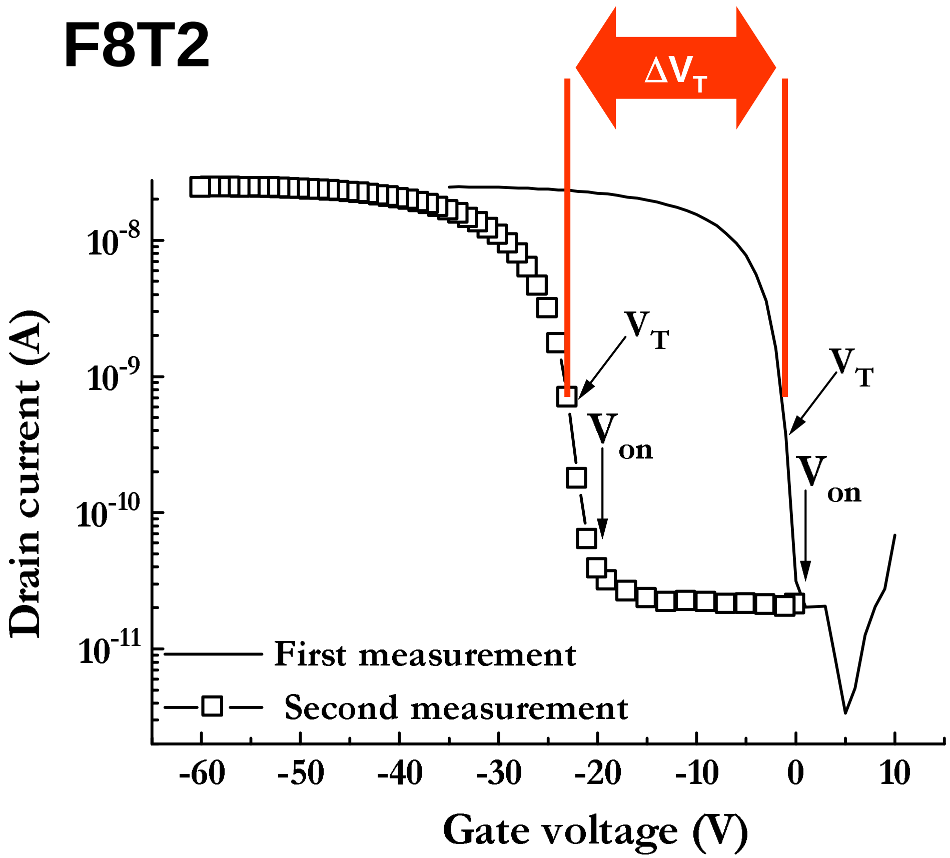
R. A. Street, A. Salleo
APL 81(5), 2887 (2002)

Threshold voltage shift during operation reduces output current

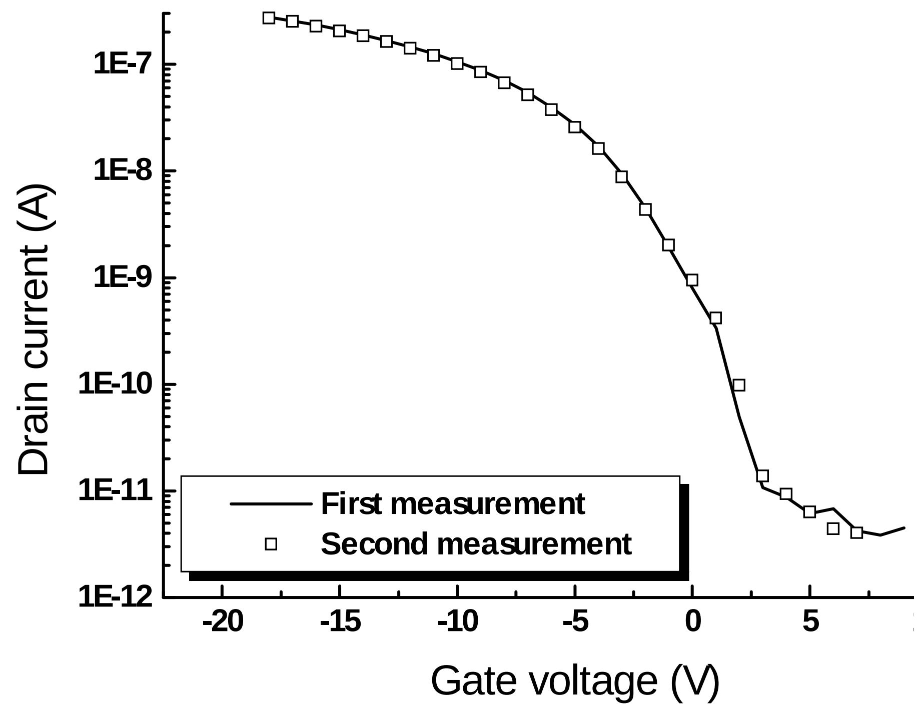


Characteristic recovery time is strongly material-dependent

F8T2



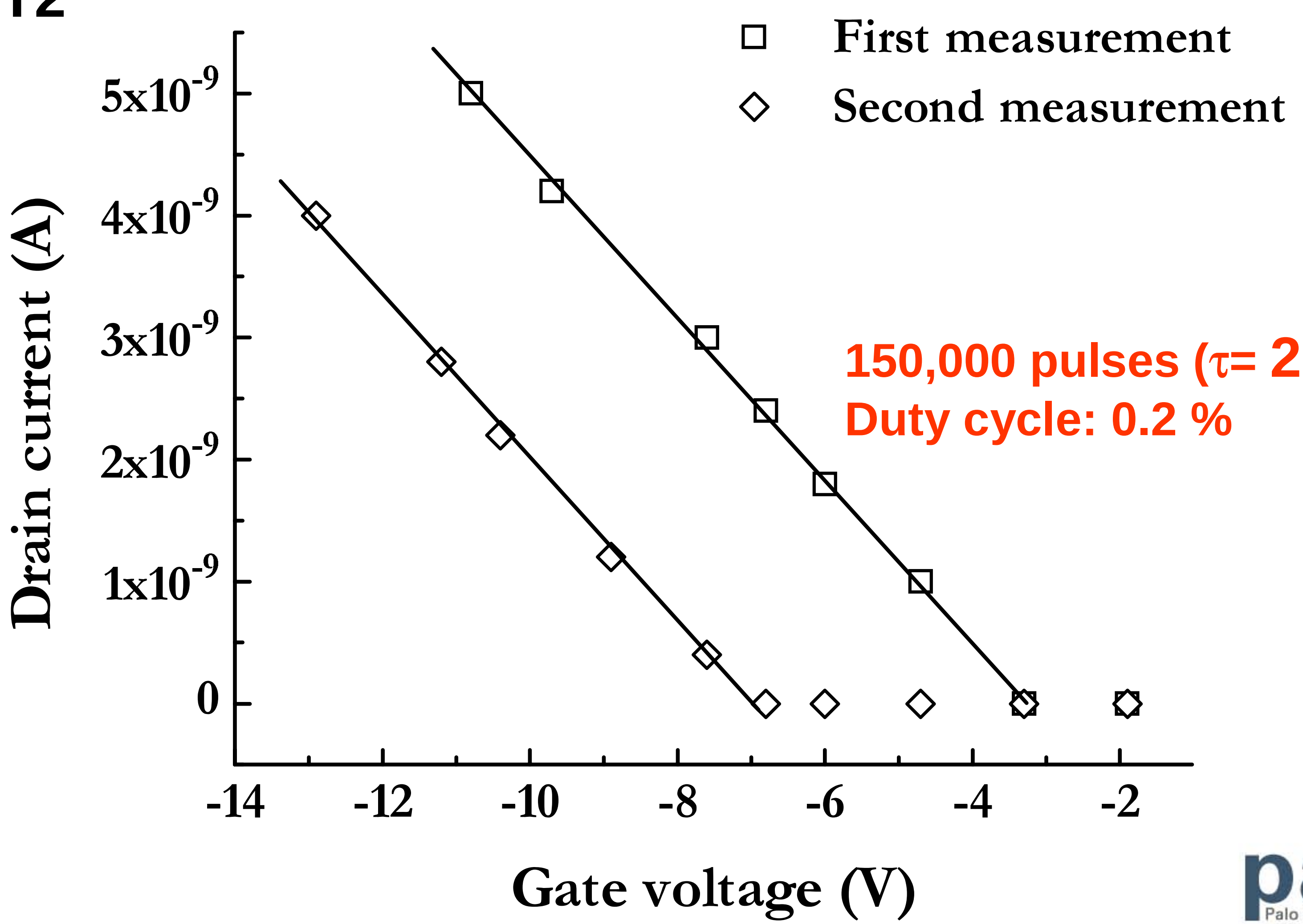
XPT



Bias stress is due to gate potential shielding by trapped charge ($=C_0\Delta V_T$)

Bias stress occurs in pulsed operation

F8T2



150,000 pulses (τ= 20 μs)
Duty cycle: 0.2 %

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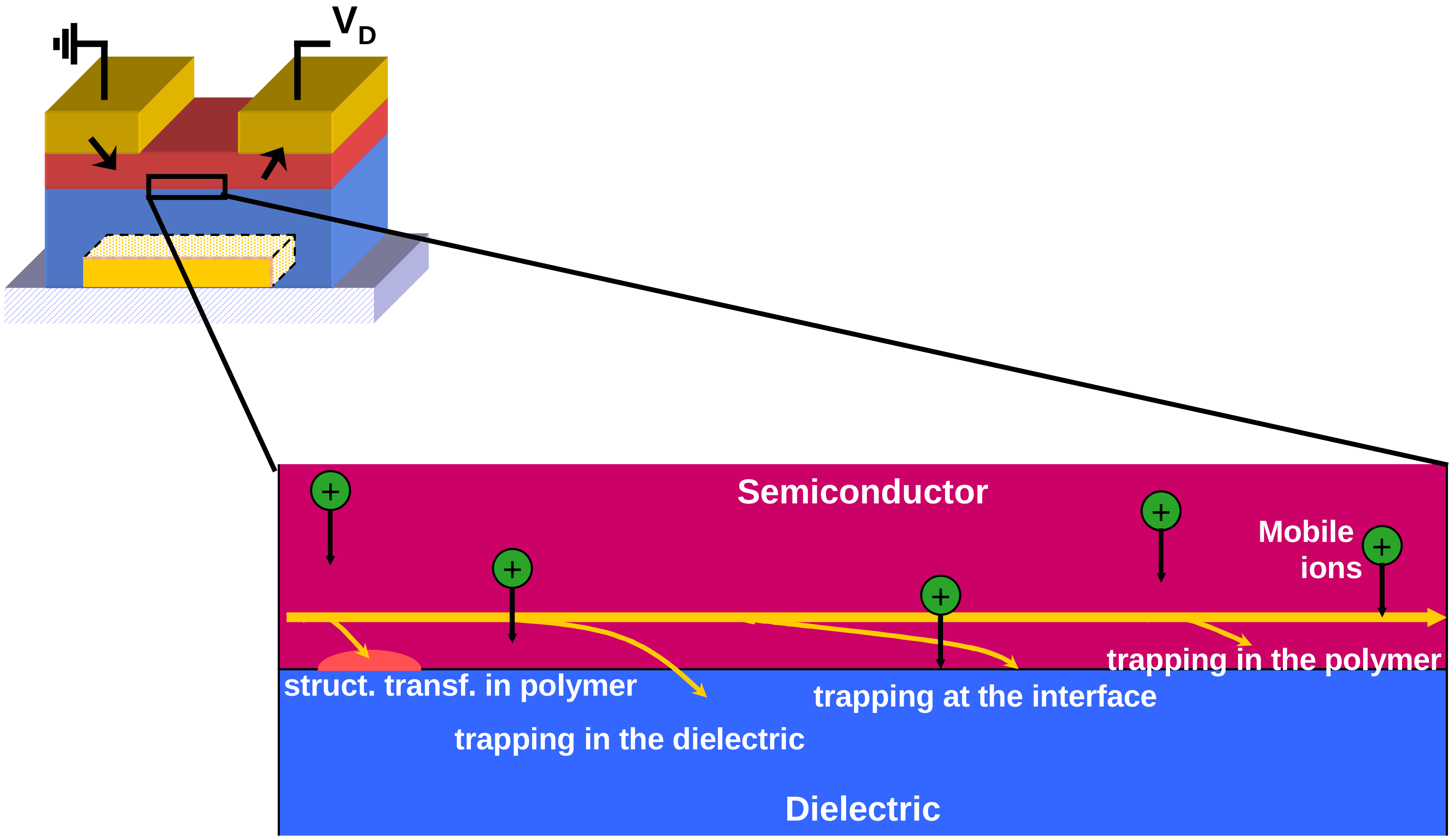
Where is the charge trapped?



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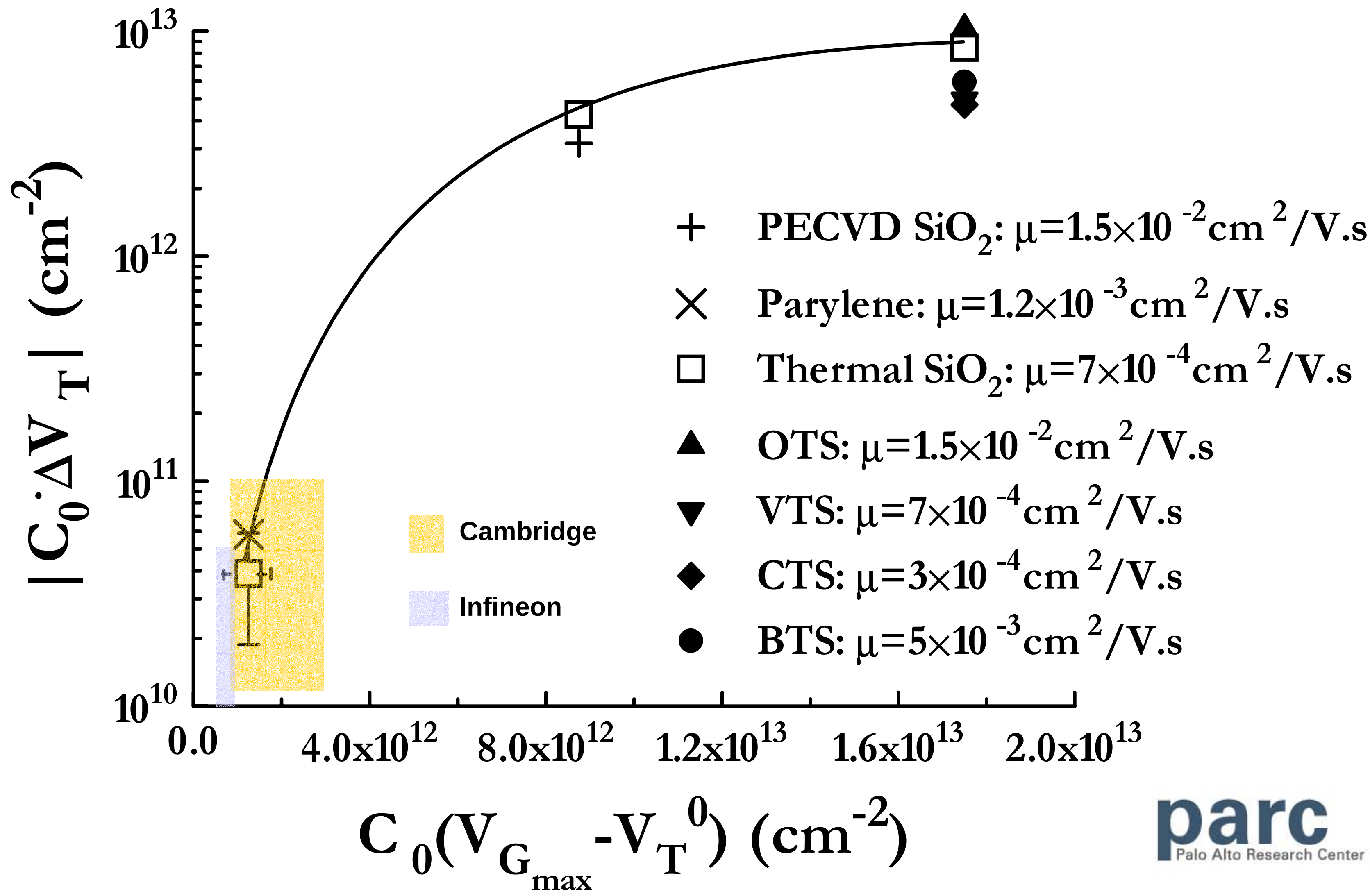
Trapping depends on effective stress not on dielectric or dielectric/semiconductor interf.

A. Salleo and R. A. Street, accepted in JAP



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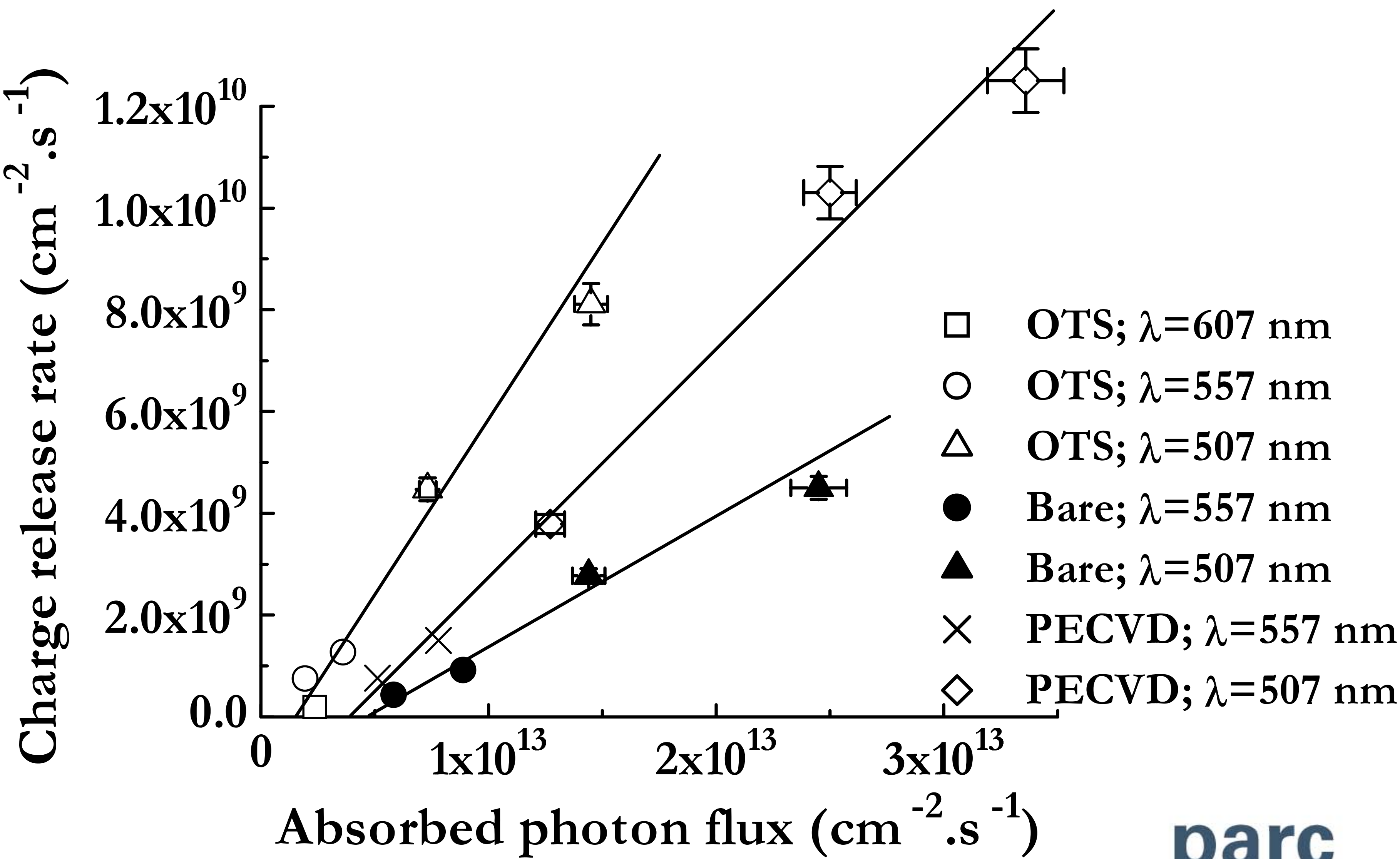
Recovery rate scales with absorption of bandgap radiation in the polymer



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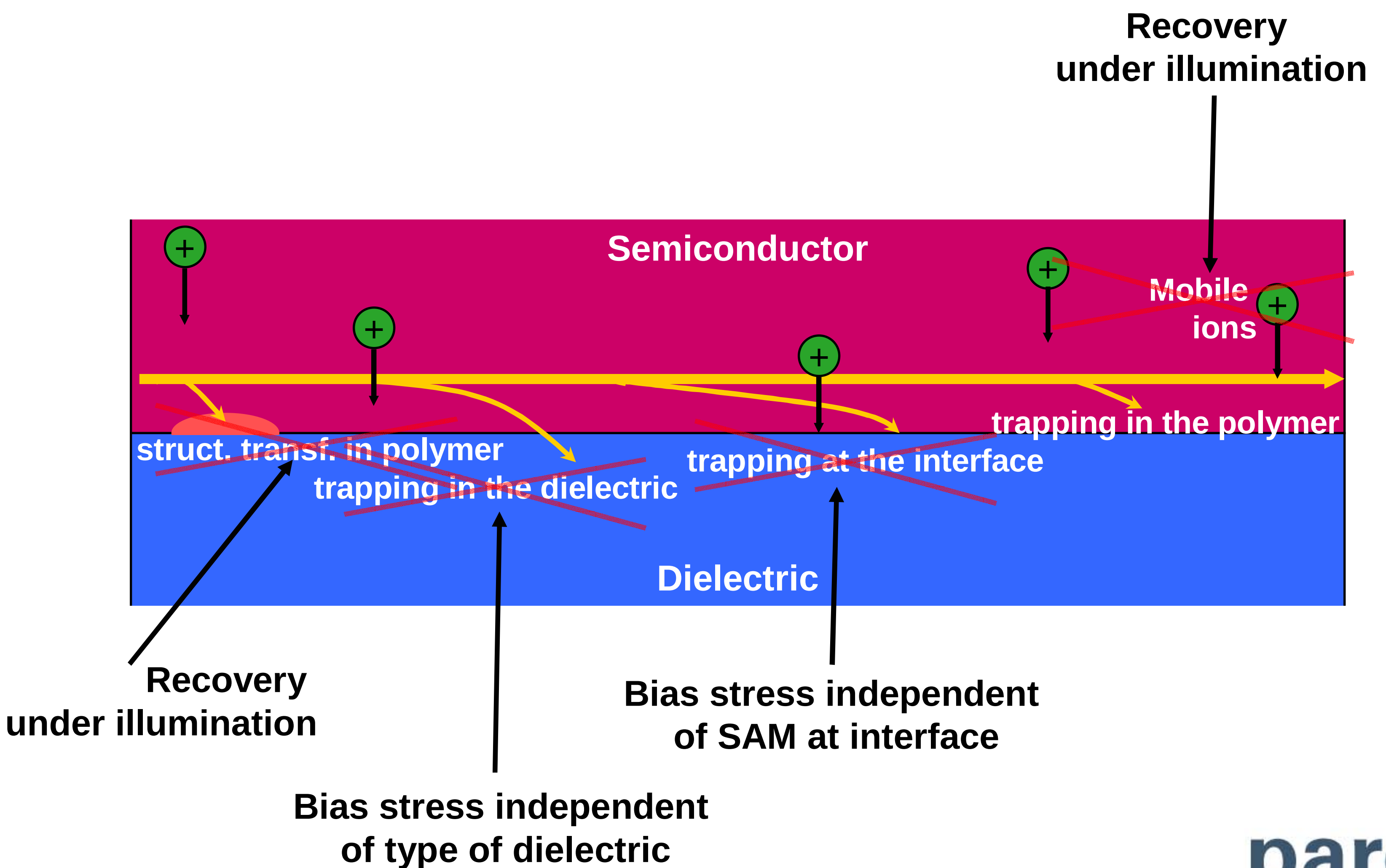
Charge trapping occurs within the polymer



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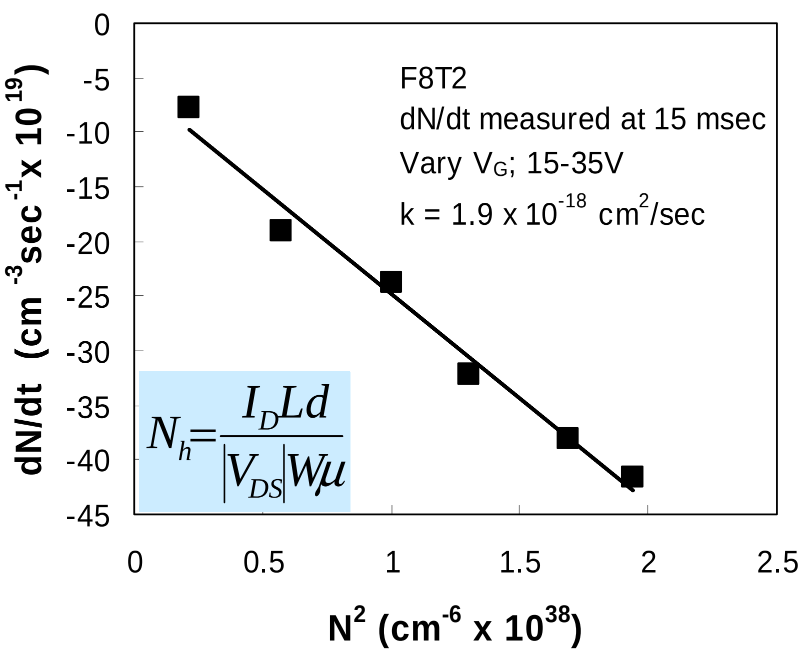
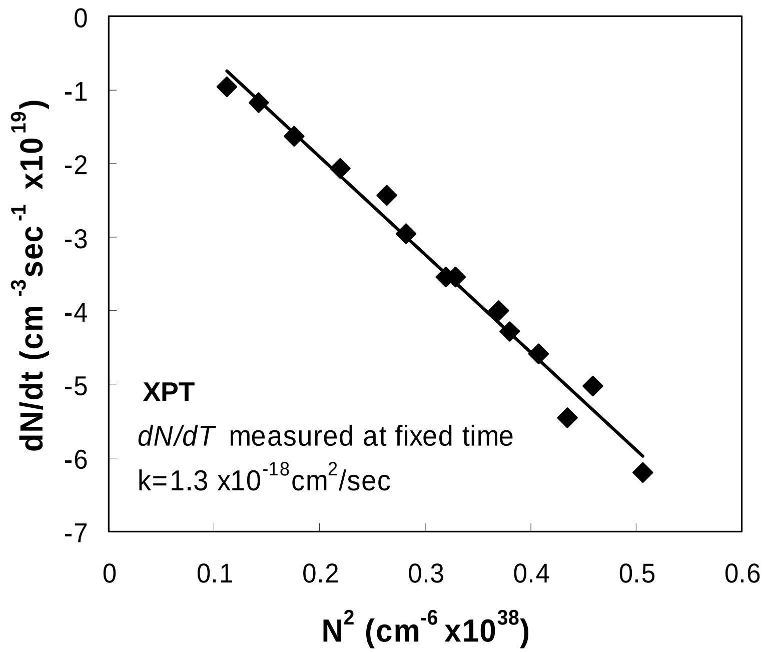
Trapping kinetic in both polymers is "bimolecular"

$$\frac{dN_h}{dt} \propto -kN_h^2$$





h + h ⟶ BP

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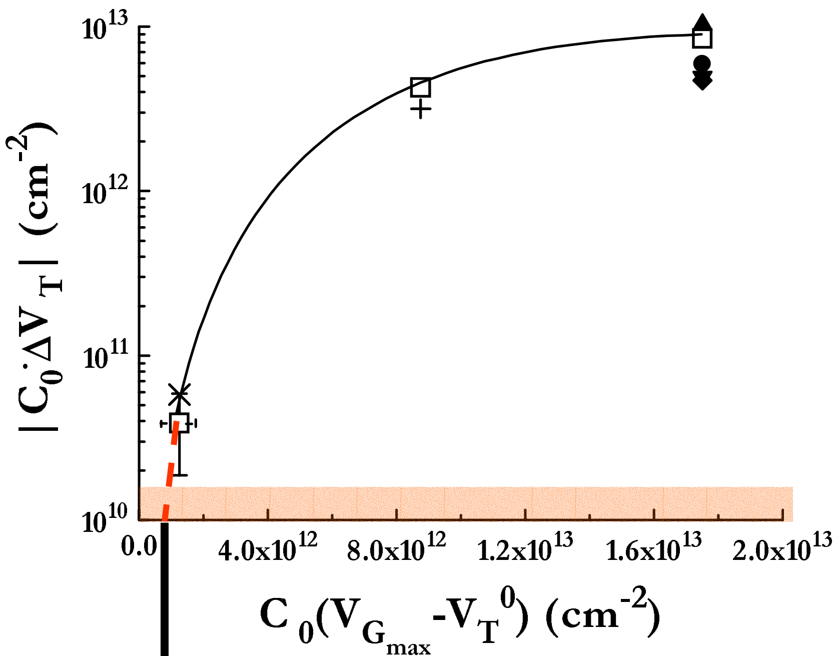
R. A. Street, A. Salleo, M. L. Chabinyc, submitted to Phys. Rev. B

Bias stress may dictate design requirements for TFTs



V_G~ -20V
V_{DS}~ -20V
I~ 1 μA
μ~ 0.015 cm²/V.s

$$\frac{W}{L} = \frac{2I}{(V_G - V_T) \times 10^{12} \times \mu} \approx 40$$

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Conclusions

- Organic electronics may enable new applications.
- Solution processing enables low-cost patterning techniques such as jet-printing.
- Polymer TFTs are approaching the properties necessary for large-area electronics.
- Control over dielectric/semiconductor interface is necessary for optimal device performance.
- Non-ideal behaviors of the material need to be understood for real applications.

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Challenges

- Organic dielectric (capacitance, compatibility, process).
- Encapsulation and via holes.
- Reliability, reproducibility and electrical stability.

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NIST ADVANCED TECHNOLOGY PROGRAM

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Michael Chabinyc
Kateri Paul
William Wong
Steve Ready
Raj Apte
Robert Street
JengPing Lu
Dietmar Knipp

Xerox Research Centre of Canada

Beng Ong
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DOW

Paul Townsend
Dave Brennan
Mitch Dibbs

MOTOROLA LABS

Dan Gamota

NIST ATP GRANT: 70NANB0H3033