

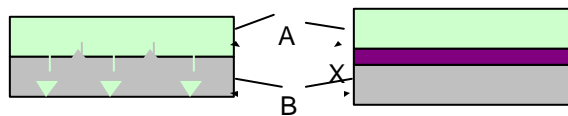
## Barriers

John Forster

Applied Materials, Inc.

## Barriers in Semiconductor Contact Metallization

Barriers are inserted between two materials to prevent them from inter-diffusing.



Desirable barrier properties: [a la M.A. Nicolet, Thin Solid Films, 52 (1978) 415.]

- diffusion of A, B through X should be small
- loss of X into A,B should be small
- X should be thermodynamically stable against A, B
- good adhesion between X to A, B
- X should be resistant to stress
- X should have good electrical, thermal conductivity

# Barriers in Semiconductor Contact Metallization

Examples of barriers in a (vintage 1983) integrated circuit.

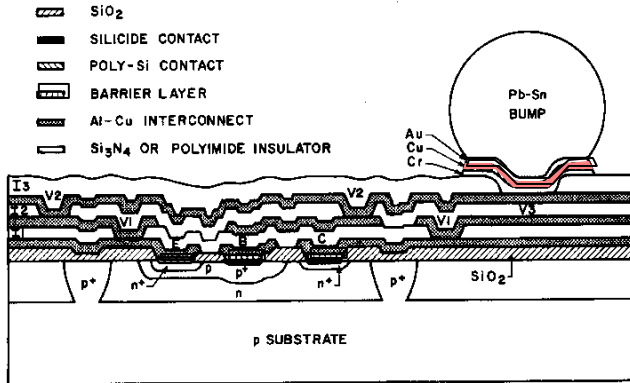


FIG. 1. Cross-sectional view of a typical VLSI metallization showing silicide and polysilicon Ohmic contacts, three levels of interconnections with vias for interlevel connections, and a solder bump for controlled collapse chip connection.

273 J. Vac. Sci. Technol. A 2 (2), Apr.-June 1984 0734-2101/84/020273-08\$01.00 © 1984 American Vacuum Society 273

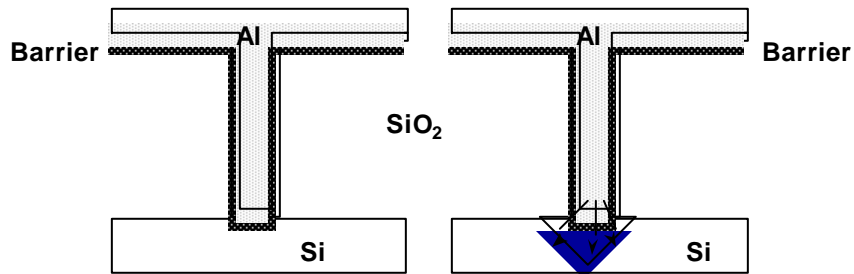
M. Wittmer, J. Vac. Sci. Technol., A2 (1984) 273

Cu, PVD & Integrated Systems



# Barriers in Semiconductor Contact Metallization

Examples: Al-barrier-Si in first level via, direct contact to Si, need to prevent "spiking" of Al into Si.



"Spiking" if Al penetrates through barrier to Si

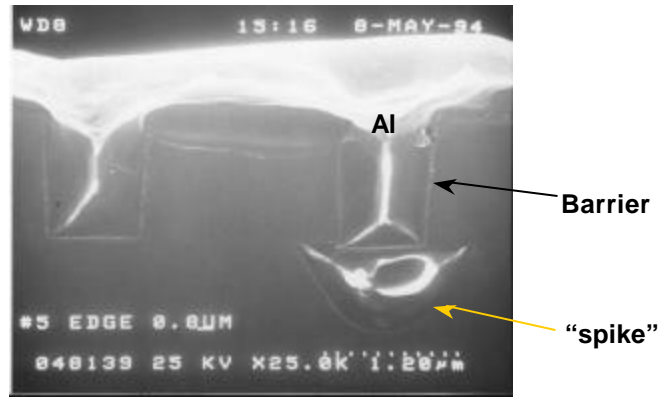
Possible barriers: TiN, TiW, W

Cu, PVD & Integrated Systems



## Barriers in Semiconductor Contact Metallization

Examples: Al – barrier – Si in first level via, direct contact to Si, failure... “spiking” of Al into Si.

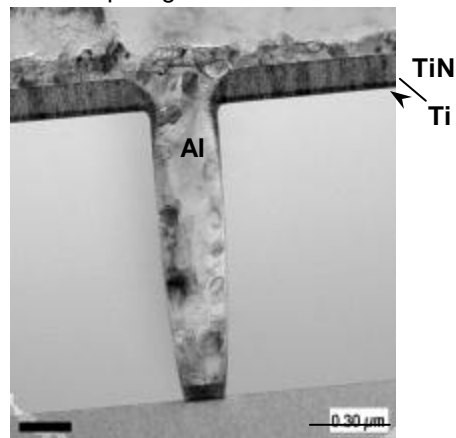


Cu, PVD & Integrated Systems



## Barriers in Semiconductor Contact Metallization

Examples: Al – barrier – Si in first level via, direct contact to Si, success...no “spiking” of Al into Si.

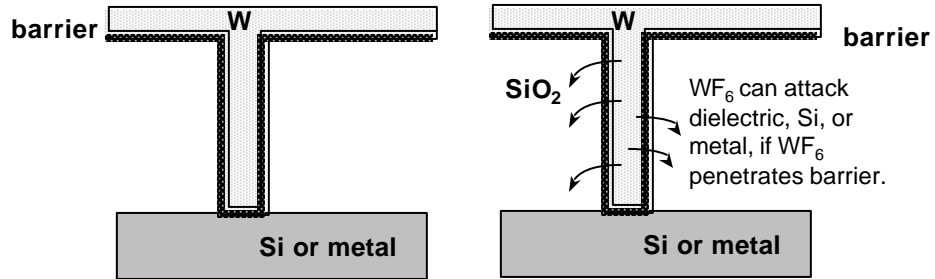


Cu, PVD & Integrated Systems



## Barriers in Semiconductor Contact Metallization

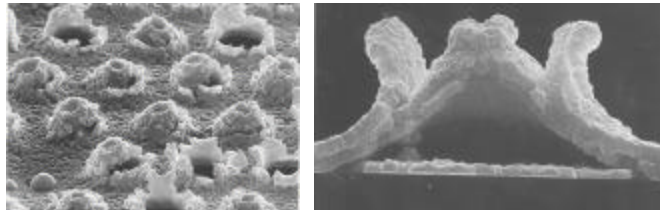
Examples:  $WF_6$  –barrier – Ti, not a diffusion barrier per se, but need to prevent  $WF_6$  attacking Ti and  $SiO_2$



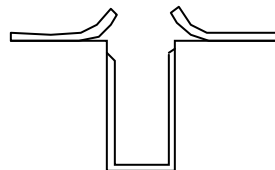
Possible barriers: TiN, W

## Barriers in Semiconductor Contact Metallization

Examples:  $WF_6$  –barrier, what happens when barrier fails...



From Tanaka et al., Proc. 5<sup>th</sup> ICSITC Conf, p207, IEEE Press, New York, 1998.



## Barriers in Semiconductor Contact Metallization

Examples:  $WF_6$  –barrier, successful barrier!



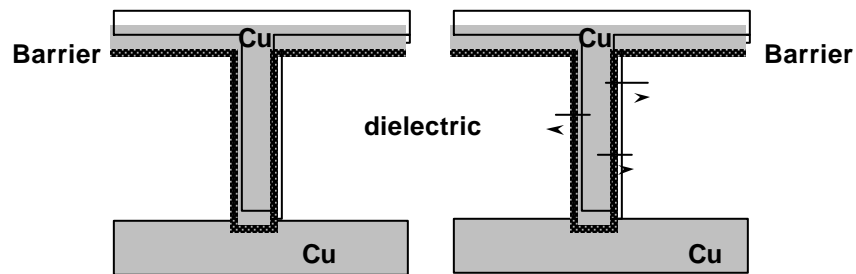
From Dixit et al.,  
IEDM Tech. Digest,  
p357, 1996.

Cu, PVD & Integrated Systems



## Barriers in Semiconductor Contact Metallization

Examples: Cu –barrier – dielectric, need to prevent diffusion of Al into dielectric.



Line leakage if Cu penetrates  
through barrier into dielectric

Possible barriers: TiN, Ta, TaN

Cu, PVD & Integrated Systems



## Barriers in Semiconductor Contact Metallization

In addition to barrier properties, barriers must also be compatible with their surroundings, e.g.

For Al – barrier – Si, Al should stick well to barrier, barrier should stick well to dielectric.

For WF6 – barrier – dielectric, W should nucleate well on barrier, and barrier should adhere well to dielectric.

For Cu – barrier – dielectric, Cu should stick well to barrier, and barrier should stick well dielectric.

In most cases, this requires barrier layers with more than one film...

## Barriers in Semiconductor Contact Metallization

Examples...”real” barriers

For Al – barrier – Si, use Ti on dielectric, then TiN (actual barrier) on Ti, then Ti layer on TiN to promote Al adhesion.

For WF6 – barrier – dielectric, use Ti on dielectric, then TiN on Ti.

For Cu – barrier – dielectric, use TaN for good adhesion to dielectric, then Ta for good adhesion to Cu.

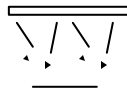
## Barriers in Semiconductor Contact Metallization

Barrier Deposition: need to consider material and deposition method

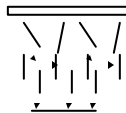
	Ti	TiN	Ta	TaN
PVD	Dominant solution	Dominant Solution?	Dominant solution	Dominant solution
CVD	Requires hi T	Dominant Solution?		
ALD			Attractive as devices shrink	Attractive as devices shrink

## Barriers in Semiconductor Contact Metallization

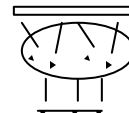
PVD Barrier Deposition: in many cases dominant solution, but requires more and more ingenuity as device dimensions shrink



Std PVD...weakly directional, up to step coverage ~1.5:1



Collimated PVD...fairly directional, up to step coverage ~3:1

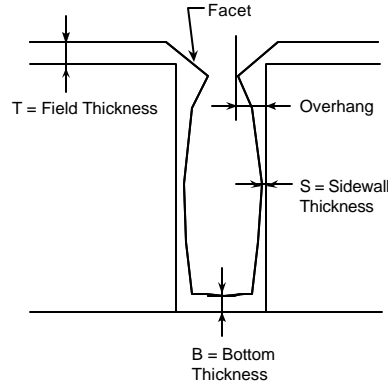


Ionized PVD...very directional, up to step coverage ~9:1

Limits to PVD?? Even if flux is highly directional, sidewall coverage is problematic, as re details with rest of structure...

## Barriers in Semiconductor Contact Metallization

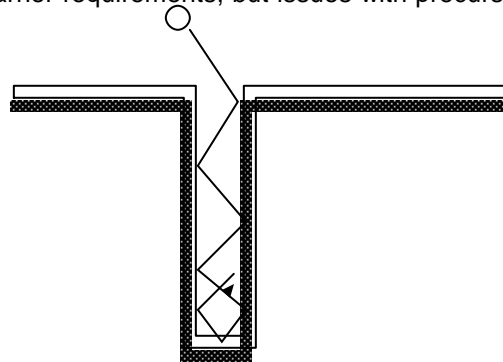
PVD Barrier Deposition: Limits to PVD lie in non-conformal step coverage.



Typical deposition profile with ionized PVD. Overhang, facet, and large difference between bottom and sidewall thickness will be ultimate limiters for PVD.

## Barriers in Semiconductor Contact Metallization

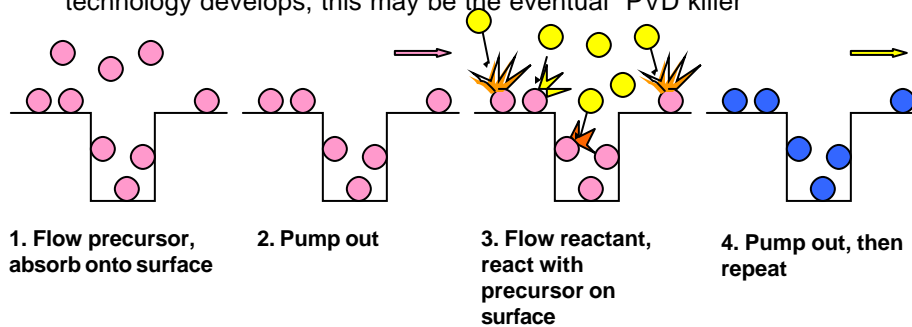
CVD Barrier Deposition: very conformal, excellent coverage for meeting barrier requirements, but issues with precursors, film purity, integration



Good conformal coverage due to low sticking coefficient. Deposition of TiN with MO-precursor has high market share, and some niche applications for high T deposition of Ti/TiN with metal halide precursor.

## Barriers in Semiconductor Contact Metallization

ALD Barrier Deposition: very conformal, excellent coverage for meeting barrier requirements, good control of film growth...as technology develops, this may be the eventual "PVD killer"



Good conformal coverage. Excellent control of film growth due to self limiting reactions on the surface. Very good performance for small, high aspect ratio features.

## Barriers in Semiconductor Contact Metallization

What makes a good barrier? Some have attempted first principles understanding...

- For a Al-barrier-Si, need a barrier that prevents diffusion, and is chemically stable towards Al and Si.
- Early barrier was  $Ti_xW_{1-x}$ , with  $x \sim 0.3$ . At temperatures above  $\sim 500^\circ\text{C}$ , Al starts to diffuse through barrier, forming  $WAl_4$  and  $WAl_{12}$ . Eventually  $W_6Si_6$  will form...barrier will fail. [Bergstrom et al., J.Appl.Phys. 82 (1997) 201.]
- Most common barrier is TiN. Not clear whether failure occurs due to diffusion of Al, Si, Ti into and through the TiN, or whether AL reacts with TiN to form AlN and  $TiAl_3$ . [J.S.Chun et al. J.Appl.Phys. 86 (1999) 3633.]

## Barriers in Semiconductor Contact Metallization

What makes a good barrier? In addition to thermodynamic properties, also look at film properties...

- Single crystalline vs polycrystalline vs amorphous..
  - Diffusion can occur along grain boundaries.
  - If film is porous, diffusion can occur between grains.
- If different atoms are placed into grain boundaries ("stuffing"), can possibly reduce diffusion.
- Experimentally, there are conflicting results on what constitutes a "good" barrier...example for TiN:
  - density of film
  - stoichiometry (metallic vs poisoned)
  - grain size
  - crystal orientation

## Barriers in Semiconductor Contact Metallization

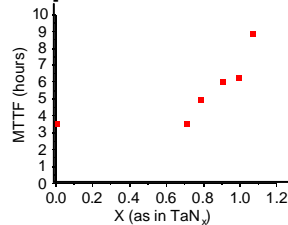
What makes a good barrier?

- For a Cu-barrier-dielectric, need a barrier that prevents diffusion, and is chemically stable towards Cu and dielectric. Good adhesion to both Cu and dielectric is also required.
- Failure is simply due to diffusion. Any material that slows diffusion can be used as a barrier: Ta, TaN, TiSiN, W, WN, even other type of dielectric.
- Selection will be driven by integration considerations, such as via resistance, resistance against stress migration and electromigration failures.
- Based on barrier and adhesion considerations, most prevalent barrier is a TaN/Ta bilayer.

## Barriers in Semiconductor Contact Metallization

What makes a good barrier?

- For a Cu-barrier-dielectric, need a barrier that prevents diffusion, and is chemically stable towards Cu and dielectric. Good adhesion to both Cu and dielectric is also required.
- There is evidence that TaN adheres better to low k dielectric, and Cu adheres better to Ta, thereby implying desirability of bilayer [D.Edelstein et al., Proc. Int. Interconn. Tech. Conf. (2001) 9].
- Experimental work exists trying to determine optimal film properties for barrier, e.g. Ta/N ratio. [from B.Sun et al. Proc Adv. Metall. Conf. (1997) 137.]



Cu, PVD & Integrated Systems



## Barriers in Semiconductor Contact Metallization

What makes a good barrier? For W applications, need

- Barrier that is resistant to  $WF_6$
- Failure occurs primarily due to insufficient coverage, cracks, or other defects in the film.
- Barrier properties are determined less by intrinsic properties, and more by deposition properties:
  - step coverage
  - density
  - freedom from cracks and other defects
  - see, e.g., G.Ramanath et al. J.Appl.Phys. 85 (1999) 1961, Tanaka et al., Proc. 5<sup>th</sup> ICSITC Conf, p207, IEEE Press, New York, 1998.

Cu, PVD & Integrated Systems

