# Modern

# SOI Materials

Jean-Pierre Colinge
University of California, Davis

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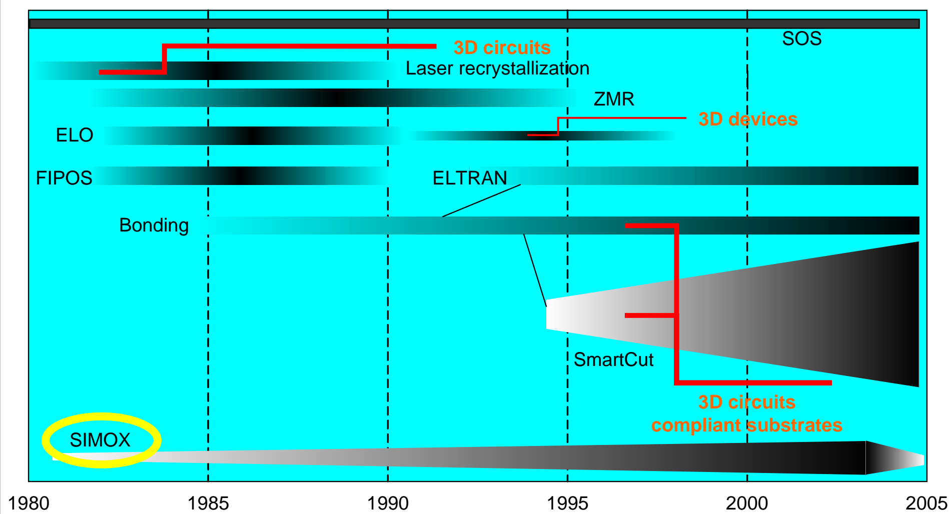
## SOI Materials

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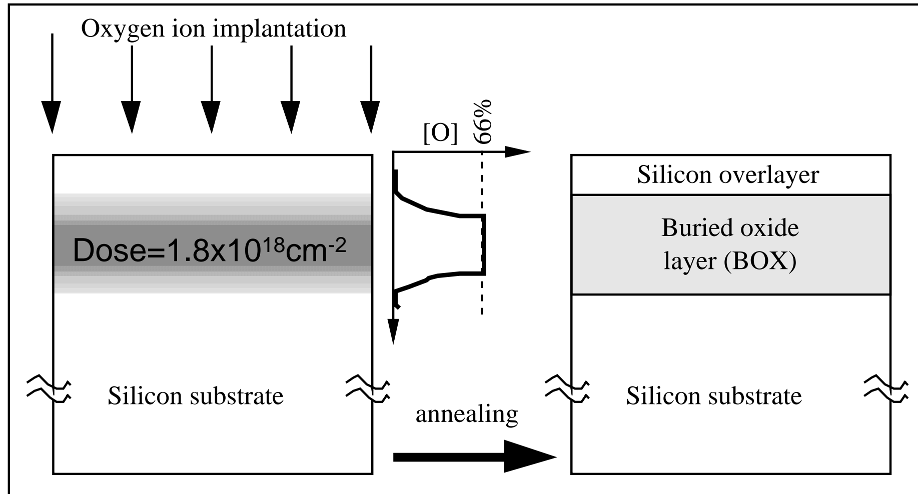
## Principle of SIMOX

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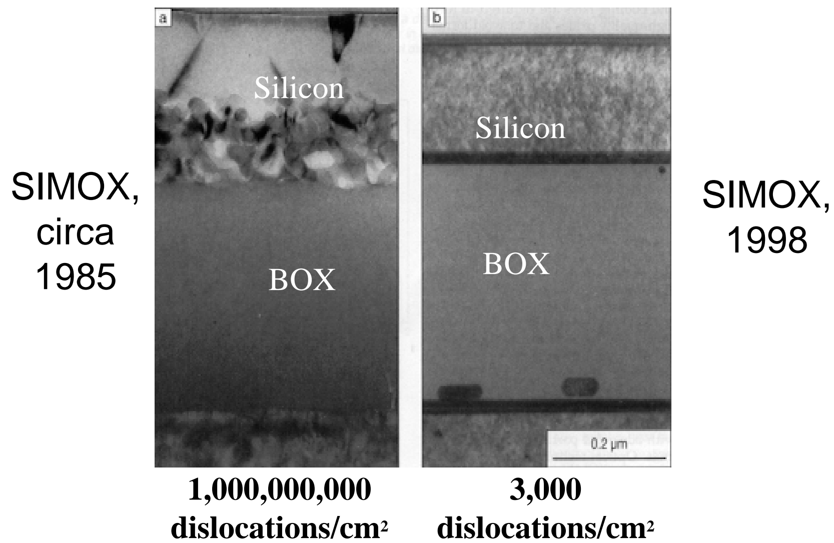
## Evolution of SIMOX quality

SIMOX, circa 1985




SIMOX, 1998

**1,000,000,000 dislocations/cm²** **3,000 dislocations/cm²**

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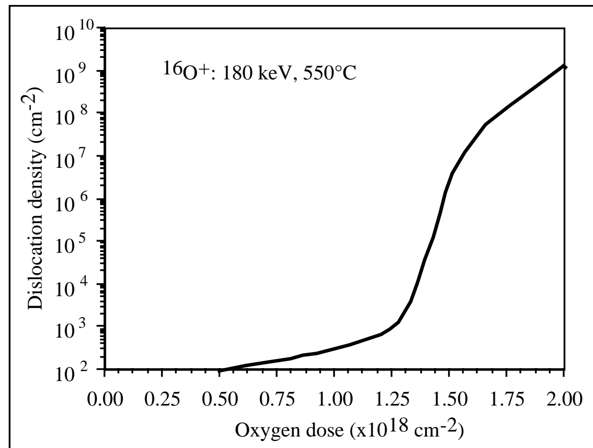
## Modified low-dose SIMOX (SIMOX-MLD)




**Evolution of dislocation density in the silicon overlayer with implanted oxygen dose**

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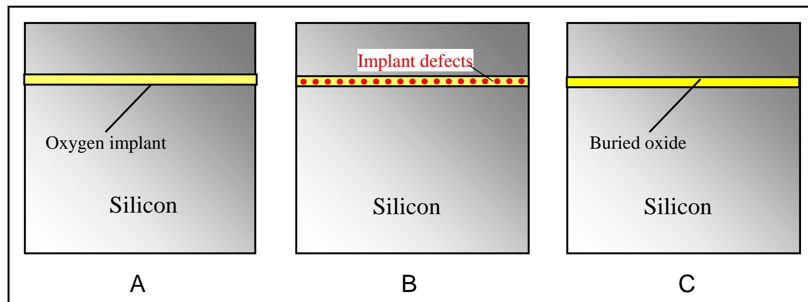
## Modified low-dose SIMOX (SIMOX-MLD)




A: First implant $3x10^{17}$ $O^+$ $cm^{-2}$, 120 keV, 525°C
B: Second implant $10^{15}$ $O^+$ $cm^{-2}$, >120 keV, room Temp.
C: Final annealing

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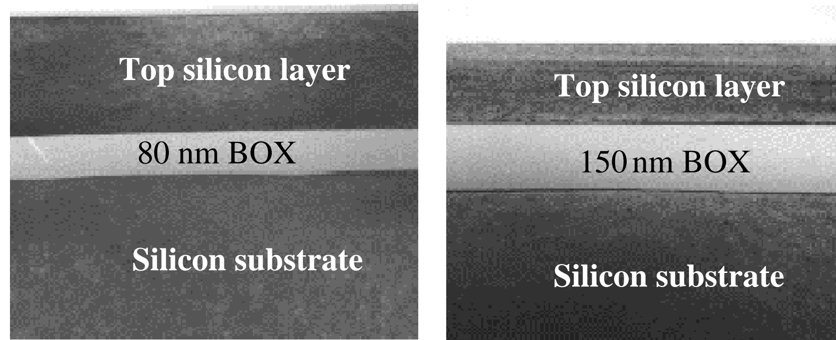
## Modified low-dose SIMOX (SIMOX-MLD)




Typical MLD: Dose=$3x10^{17}cm^{-2}+10^{15}cm^{-2}$

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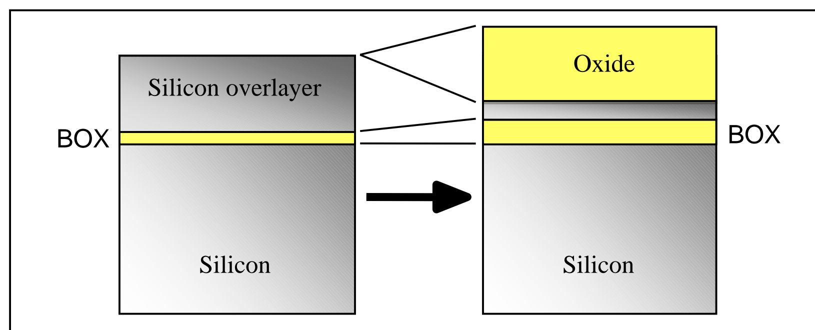
## Variations on the SIMOX theme: ITOX




**Principle of internal thermal oxidation (ITOX)**

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# SIMOX material properties

| **Parameter** | Standard SIMOX | SIMOX MLD |
|---|---|---|
| Wafer diameter | up to 200 mm | up to 300 mm |
| Silicon film thickness | 210 nm | 20 to 145 nm |
| Silicon film thickness uniformity | | ±2 nm |
| Buried oxide (BOX) thickness | 375 nm | 135, 145 nm |
| Buried oxide (BOX) thickness uniformity | ±10 nm | ±5 nm |
| Surface roughness (RMS) | 0.7 nm | <0.15 nm |
| Dislocation density | < 1000 $cm^{-2}$ | < 1000 $cm^{-2}$ |
| HF defect density | < 0.5 $cm^{-2}$ | < 0.1 $cm^{-2}$ |
| BOX pipe (pinhole) density | < 0.1 $cm^{-2}$ | < 0.1 $cm^{-2}$ |
| Metallic contamination | < $5x10^{10}$ $cm^{-2}$ | < $3x10^{10}$ $cm^{-2}$ |
| BOX dielectric breakdown | >5 MV/cm | >7 MV/cm |

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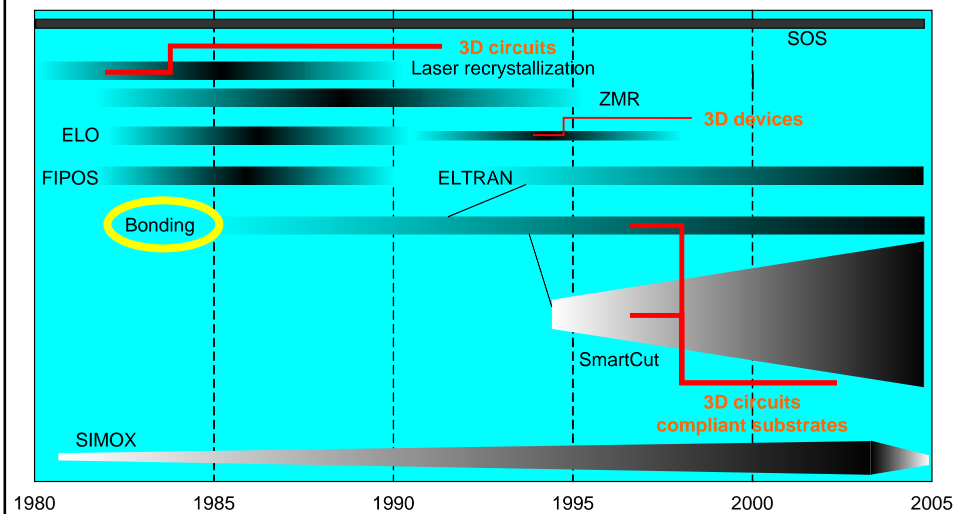
# SOI Materials

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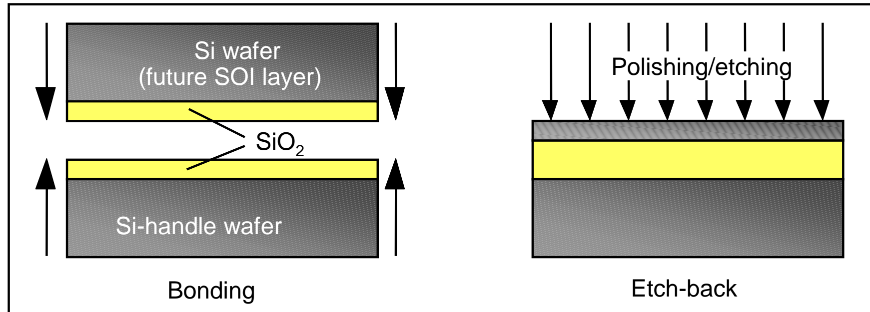
## Bonded and Etch-back SOI (BESOI)




Bonding of two oxidized silicon wafers (left) and polishing/etching back of one of the wafers

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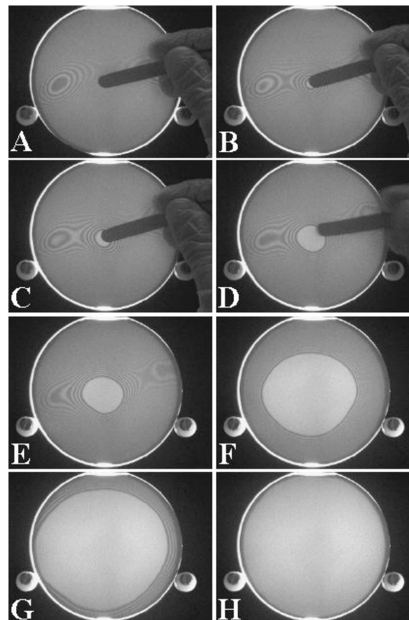
## Bonding mechanism

**Infrared transmission imaging showing the propagation of a bonding wave between two oxidized 100-mm silicon wafers (from A to H). Time between different pictures is approximately 0.5 second.**




**Movie can be viewed at:**
http://www.waferbond.com/

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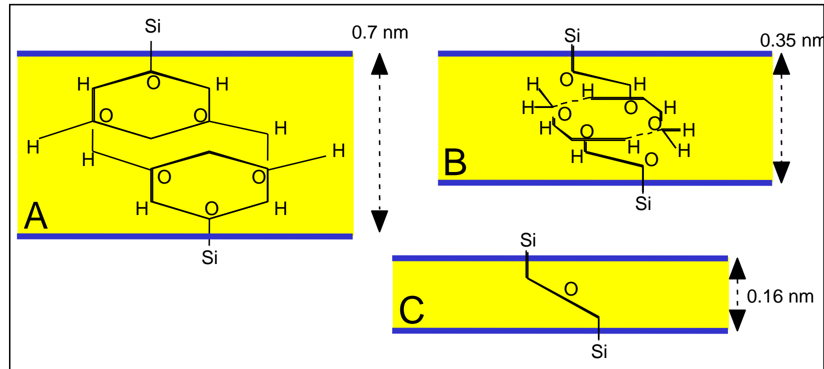
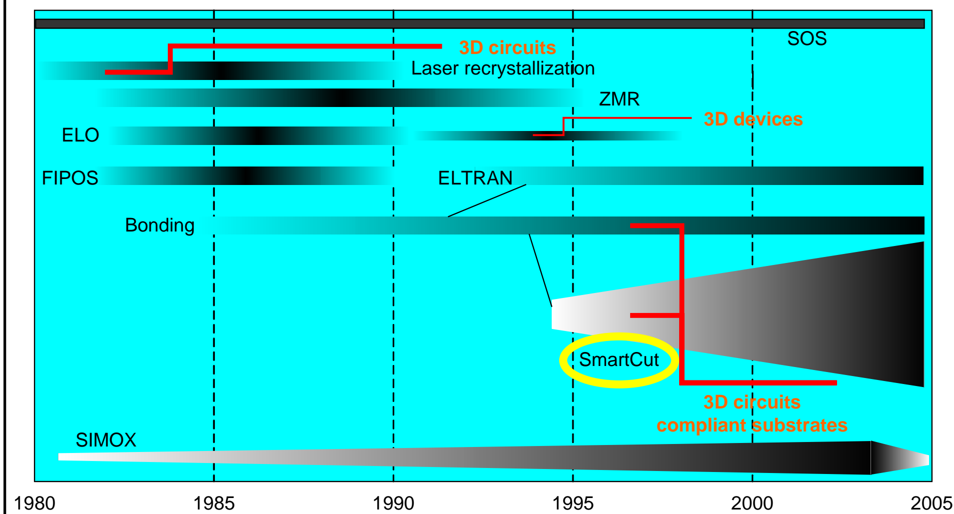
## Stengl's model for silicon wafer bonding



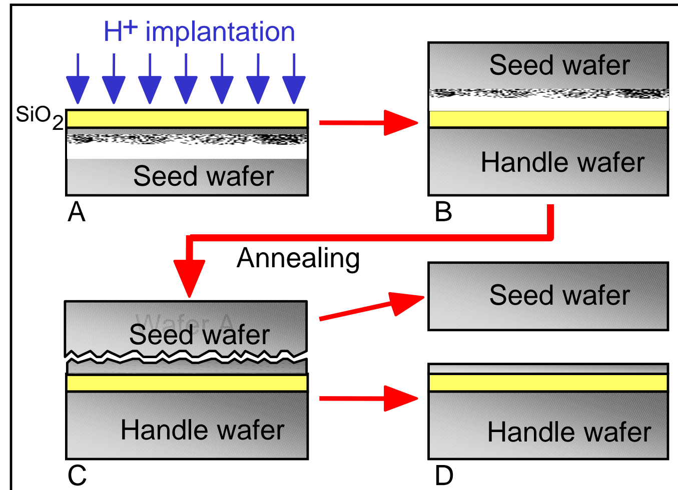

A: Room temperature, $SiOH:(OH_2)_2:(OH_2)_2:HOSi$;
B: T = 200°C, $SiOH:HOSi + (H_2O)_4$
C: T > 700°C, $SiOSi + H_2O$



## SOI Materials



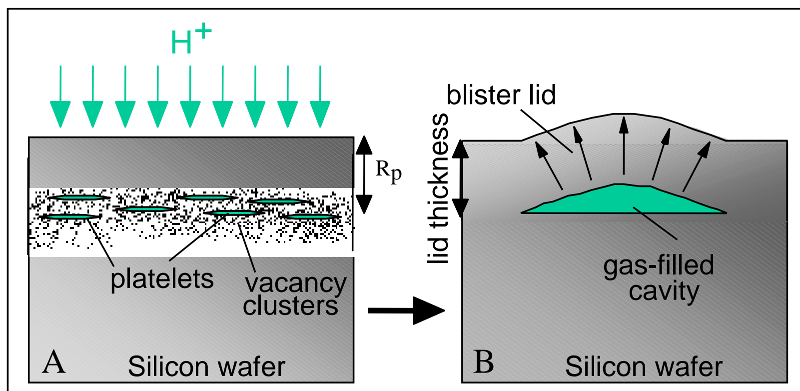
## Smart-Cut® process




A: Hydrogen implantation; B: Wafer bonding; C: Splitting of wafer A; D: Polishing of both wafers. Wafer A is recycled as a future handle wafer

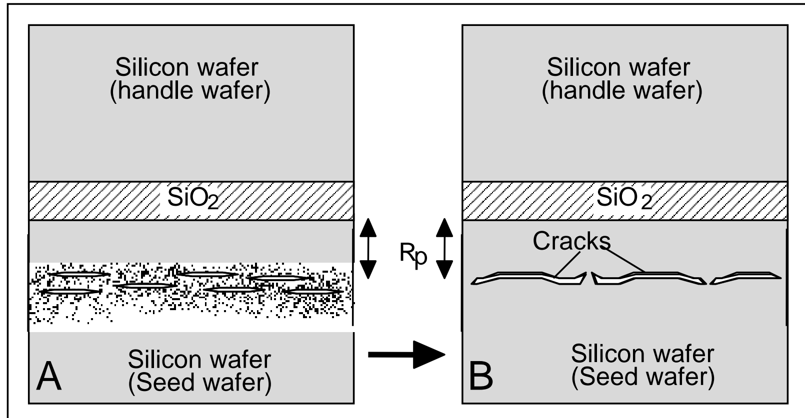


## Smart-Cut® process




A: Hydrogen implantation ad formation of defects (vacancies, vacancy clusters and platelets); B: Formation of a blister upon annealing. $R_p$ is the projected range of the implanted ions.

## Smart-Cut® process




Formation of cracks near the projected range of s silicon wafer implanted with hydrogen. A: Bonding of the handle wafer (stiffener) to the seed wafer; B: Formation of a crack network near the projected range upon annealing.

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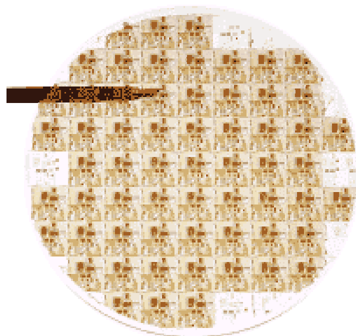
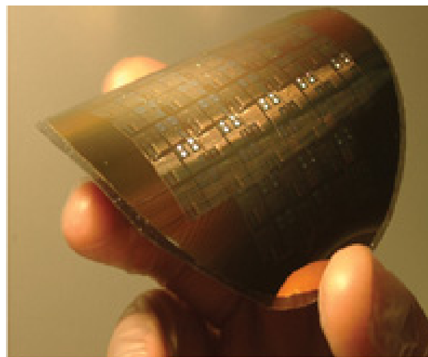
## Layer transfer using bonding Techniques



SOI devices transferred onto 200 mm fused silica wafer



Bulk devices thinned down to 35 µm and transferred onto a plastic film

http://www.tracit-tech.com/transfer.html

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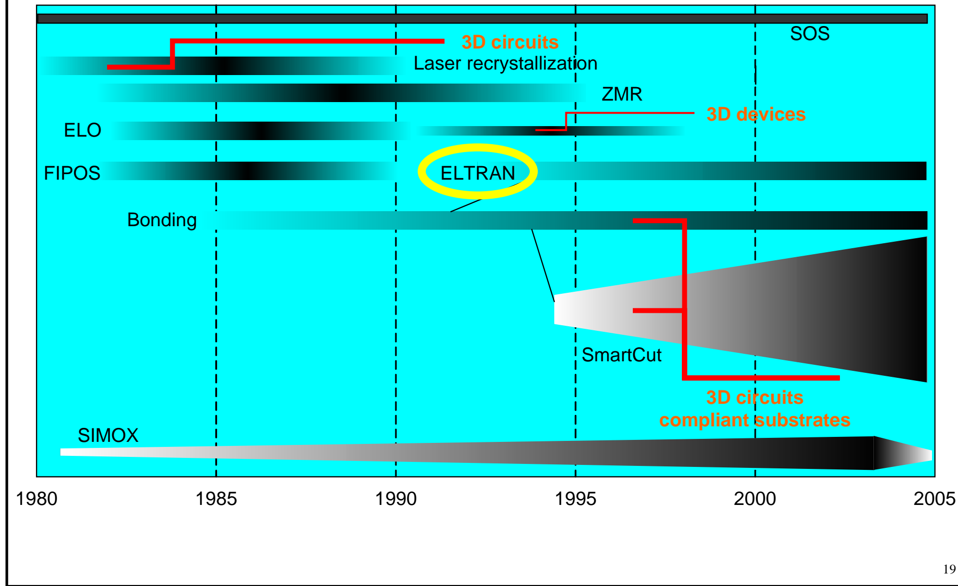
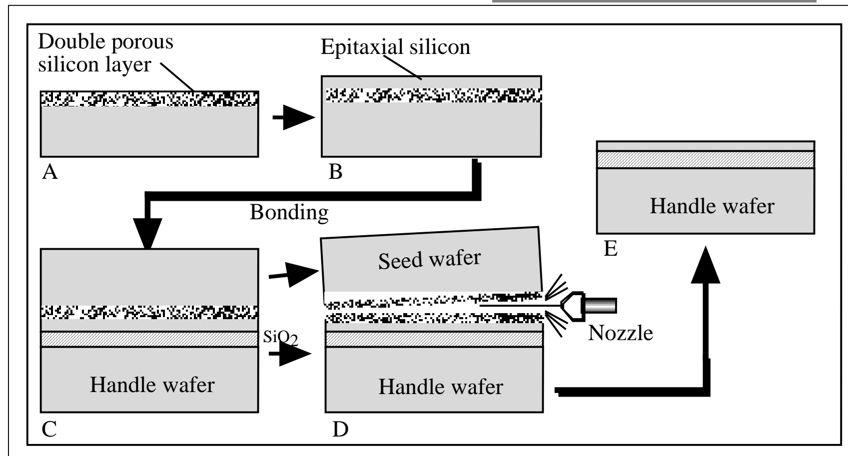
# SOI Materials






# Eltran® process




A: Formation of a porous silicon layer by electrochemical reaction in HF; B: Growth of epitaxial silicon; C: Bonding to a handle wafer; D: Porous silicon layer splitting using a water jet; E: Etching and $H_2$ annealing.

## Eltran® process

Wafer pair

Nozzle

http://www.canon.com/technology/detail/device/soi/

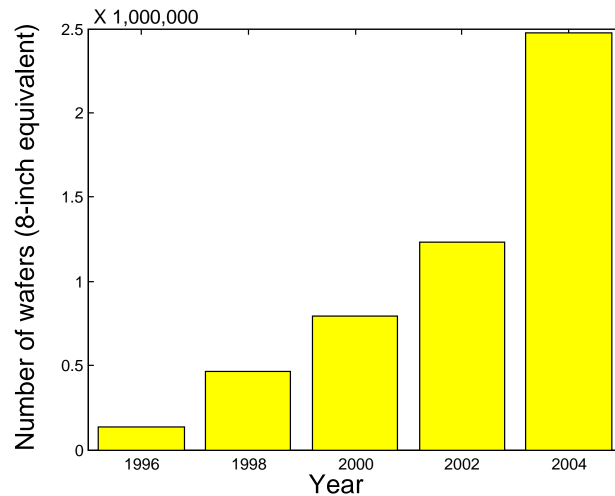
http://www.mrs.org/meetings/spring2001/presentations/SO1I8.2_color.pdf



## Transferred layer material properties

| Parameter | Unibond® | Eltran® |
|---|---|---|
| Wafer diameter | 300 mm | 300 mm |
| Silicon film thickness | 50 to 100 nm | 20 to 145nm |
| Silicon film thickness uniformity | ± 0.5 nm | ±1.6 nm |
| Buried oxide (BOX) thickness | 100 nm to 3 μm | 135, 145 nm |
| Buried oxide thickness uniformity | ±0.1 nm | ±2 nm |
| Surface roughness (RMS) | 0.15 nm | 0.1 nm |
| Dislocation density | 100 $cm^{-2}$ | 400 $cm^{-2}$ |
| HF defect density | 1 $cm^{-2}$ | < 0.05 $cm^{-2}$ |
| BOX pipe (pinhole) density | none | none |
| Metallic contamination | $5x10^{10}$ $cm^{-2}$ | $5x10^{10}$ $cm^{-2}$ |

Estimated worldwide SOI wafer production capability

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# SOI CMOS Processing and Design Issues


Jean-Pierre Colinge
University of California, Davis


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# Outline

- Evaluation of SOI wafers
- Process-related metrology issues
- SOI vs. bulk CMOS processing
- Process steps and processing issues specific to SOI

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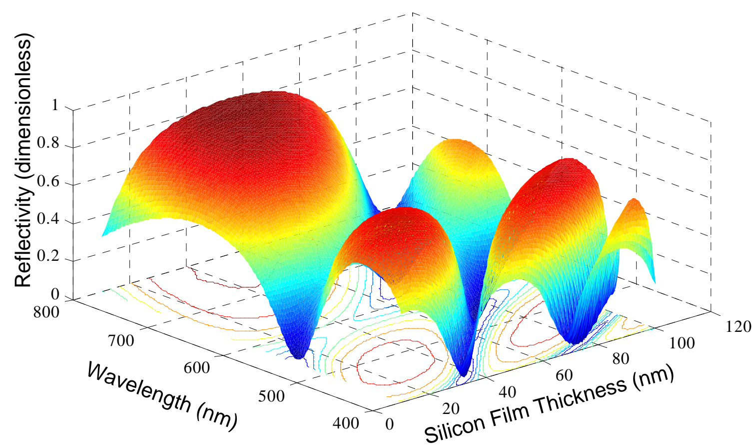
## Thickness measurement/Reflectometry




Reflectivity of the SOI structure as a function of wavelength and silicon film thickness. The BOX thickness is 400 nm.

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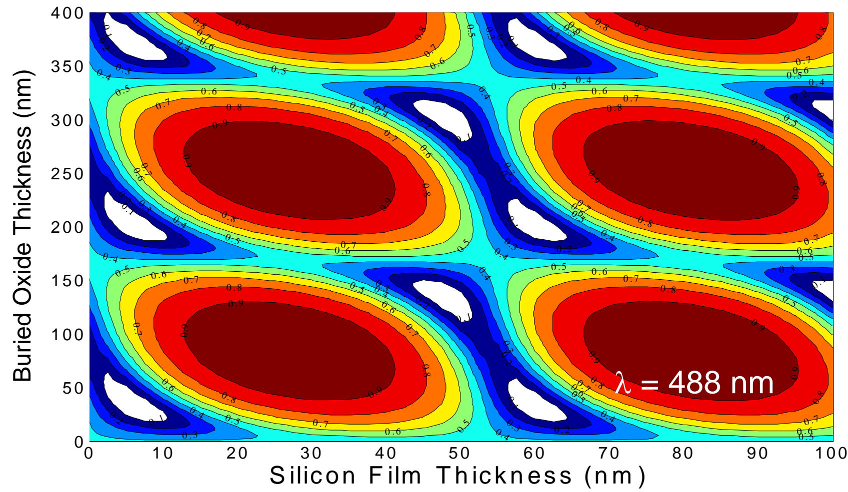
## Metrology issue: haze/particulate detection




Apparent particulate size depends on reflectivity !

C. Maleville, E. Neyret, L. Ecarnot, T. Barge, A.J. Auberton, Proceedings of the IEEE International SOI Conference, p. 19, 2001
C. Maleville, Electrochemical Society Proceedings Vol. 2003-05, p. 33, 2003
C. Maleville, C. Moulin, E. Neyret, Proceedings of the IEEE International SOI Conference, p. 194, 2002



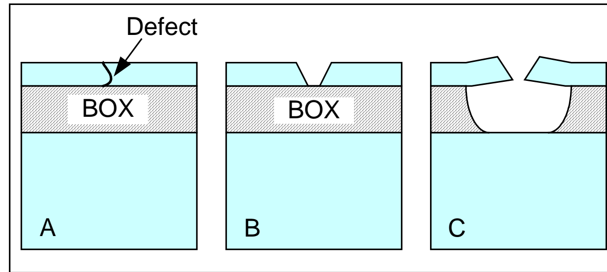
## Chemical decoration of defects

| | |
|---|---|
| Dash etch | $HF:HNO_3:CH_3COOH$ 1:3:10 |
| Schimmel etch | HF:1M $CrO_3$ 2:1 |
| Secco etch | HF:0.15M $K_2Cr_2O_7$ 2:1 |
| Stirl etch | HF:5M $CrO_3$ 1:1 |
| Wright etch | 60ml HF:30 ml $HNO_3$:30 ml 5M $CrO_3$: 2 grams $Cu(NO_3)_2$:60 ml $H_2O$ |
| Electrochemical etch | 5% wt HF |
| Iodine etch | 2M KI:0.5M $I_2$:2.5M HF:28.5M $CH_3OH$:66.5M $H_2O$ |

W.C. Dash, J. Appl. Phys, Vol. 27, p. 1993, 1956
D.G. Schimmel, J. Electrochem. Soc, Vol. 126, p. 479, 1979
F. Secco d'Aragona, J. Electrochem. Soc., Vol. 119, p. 948, 1972
E. Sirtl and A. Adler, Zeitung für Metallkunde, Vol. 52, p. 529, 1961
M. Wright Jenkins, J. Electrochem. Soc., Vol. 124, p. 757, 1977
T.R. Guilinger, M.J. Kelly, J.W. Medernach, S.S. Tsao, J.O. Steveson, and H.D.T. Jones, Proceedings of the IEEE SOS/SOI Technology Conference, p. 93, 1989
M.J. Kelly, T.R. Guilinger, J.W. Medernach, S.S. Tsao, H.D.T. Jones, and J.O. Steveson, Electrochemical Society Proceedings, Vol. 90-6, p. 120, 1990
K. Imamura, K. Daido, K. Mimegishi, H. Nakanishi, Japanese Journal of Applied Physics, Vol.16, suppl.1, p. 547, 1977
Y. Moriyasu, T. Morishita, M. Matsui, A. Yasujima, M. Ishida, Electrochemical Society Proceedings, Vol. 99-3, p. 137, 1999

## Chemical decoration of defects

Problem: Si film may be too thin and is etched before defects are decorated.




Defect in thin SOI layer (A) revealed by Secco etch (B) followed by HF etch (C)

H. Moriceau, B. Aspar, M. Bruel, A.M. Cartier, C. Morales, A. Soubie, T. Barge, S. Bressot, C. Maleville, A.J. Auberton, Electrochemical Society Proceedings, Vol. 99-3, p. 173, 1999

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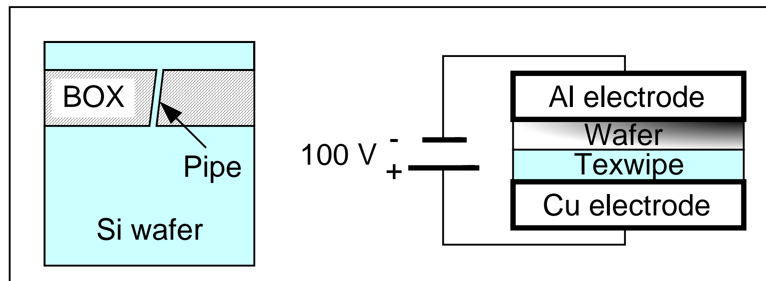
## Chemical decoration of BOX pipes




The electrolytic reaction $CuSO_4 \rightarrow Cu^{++} + SO_4^-$ and $Cu^{++} + 2e^- \rightarrow Cu(s)$ takes place in the Texwipe™ wherever it receives current from a pipe. Stains (dots) of metallic copper are, therefore, created on the Texwipe™, each corresponding to a pipe in the BOX

L.P. Allen, M.J. Anc, M. Duffy, J.H. Parechanian, J.H. Yap, Electrochemical Society Proceedings Vol. 96-3, p. 18, 1996

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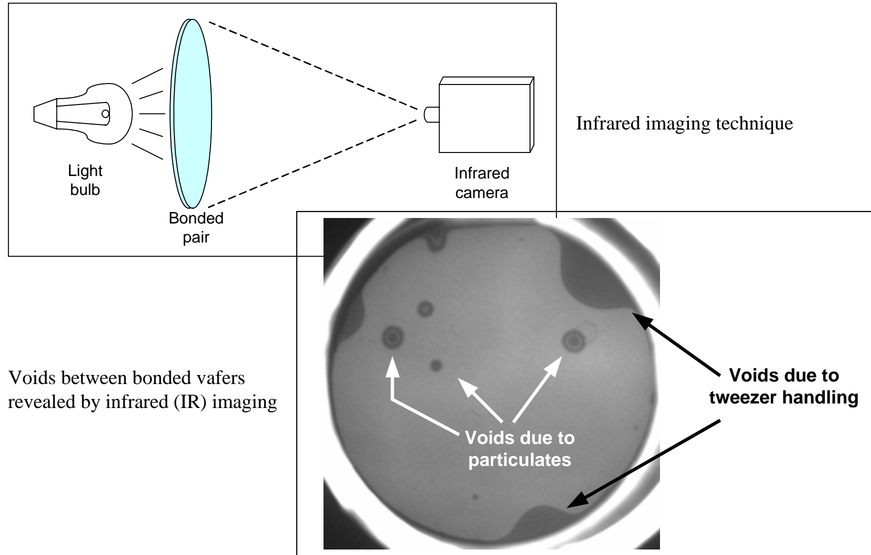
# Wafer Bonding Quality




Infrared imaging technique

Voids between bonded vafers revealed by infrared (IR) imaging

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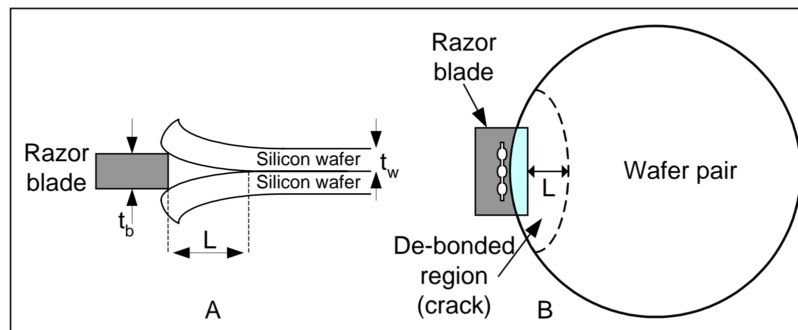
# Bonding Strength




Crack propagation measurement; A: lateral view; B: top view

The strength of the bond (or bonding energy) is measured in erg/cm$^2$ or J/m$^2$ (1 erg/cm$^2$ = $10^{-3}$ J/m$^2$). The most common technique used to measure bond energy is the so-called "crack propagation technique" based on the insertion of a razor blade between the bonded wafers (Figure 3.12). The insertion of a blade of thickness $t_b$ causes the formation of a "crack" or a de-bonded region that extends over a length $L$ past the edge of the blade. The extension of the crack can be measured by infrared imaging. The bond energy, $\gamma$, is given by:

$$\gamma = \frac{3 E t_w^3 t_b^2}{32 L^4} \quad \text{(J/m}^2\text{)}$$

where $t_w$ is the thickness of each individual wafer (m), $E$ is the silicon Young's modulus (166 GPa) and $L$ is the crack length (m). This measurement is very easy to perform, but any inaccuracy in measuring the crack length induces large variations of the calculated bonding energy, because of the fourth-power dependence of $\gamma$ on $L$. A 10% inaccuracy in crack length measurement, for instance, leads to a near 50% error in bonding energy.


W.P. Maszara, G. Goetz, A. Caviglia, J.B. McKitterick, Journal of Applied Physics, Vol. 64, p. 4943, 1988
Q.Y. Tong and U. Gösele, *Semiconductor Wafer Bonding Science and Technology*, The Electrochemical Society Series, John Wiley & Sons, p. 25, 1999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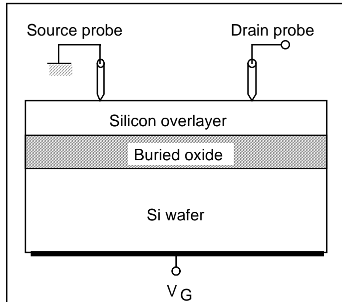
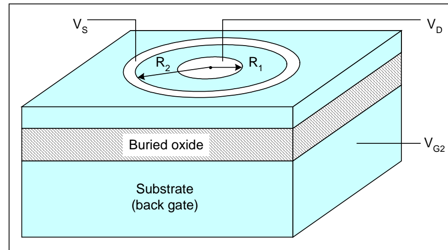
## Ψ-MOSFET




Principle of the Ψ-MOSFET




Ψ-MOSFET with circular, concentric source and drain electrodes

$$I_D = f_g C_{ox2} \frac{\mu_o}{1+\theta(V_{G2}-V_{T2/FB2})}(V_{G2}-V_{T2/FB2})V_D$$

$$I_D = \frac{2\pi}{\ln(R_2/R_1)}\mu C_{ox}\left(V_{G2}-V_{TH2/FB2}\right)V_D$$


S. Cristoloveanu and S. Williams, IEEE Electron Device Letters, Vol. 31, p. 102, 1992
S. Cristoloveanu and S.S. Li, *Electrical Characterization of Silicon-On-Insulator Materials and Devices*, Kluwer Academic Publishers, p. 104, 1995
D. Munteanu, S. Cristoloveanu, and H. Hovel, Electrochemical and Solid-State Letters, Vol. 2, p. 242, 1999.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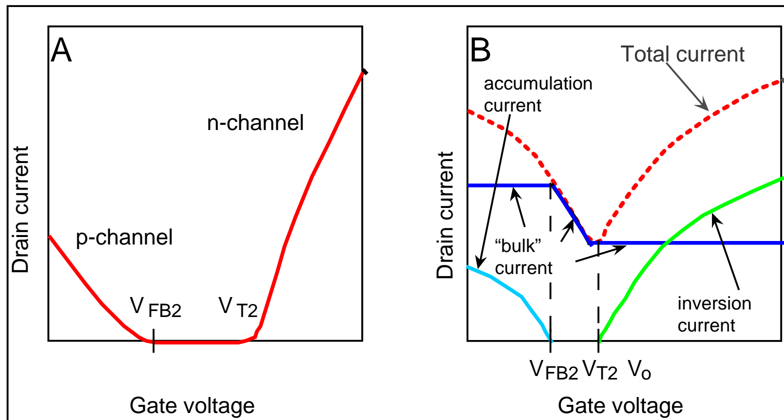
## Ψ-MOSFET




I-$V_G$ characteristics of a Ψ-MOSFET. A: fully depleted film; B: partially depleted film


S. Cristoloveanu and S. Williams, IEEE Electron Device Letters, Vol. 31, p. 102, 1992
S. Cristoloveanu and S.S. Li, *Electrical Characterization of Silicon-On-Insulator Materials and Devices*, Kluwer Academic Publishers, p. 104, 1995
D. Munteanu, S. Cristoloveanu, and H. Hovel, Electrochemical and Solid-State Letters, Vol. 2, p. 242, 1999.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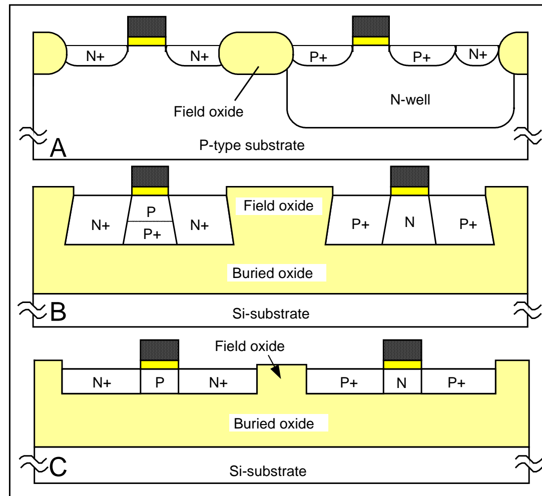
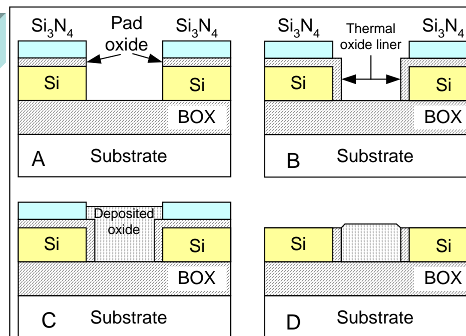
# CMOS Processing



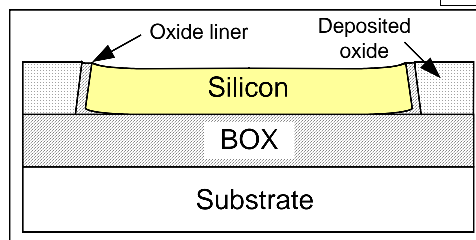

Cross-section of
A: bulk CMOS inverter
B: partially depleted SOI CMOS inverter, and
C: fully depleted SOI CMOS inverter



# Shallow Trench Isolation (STI)



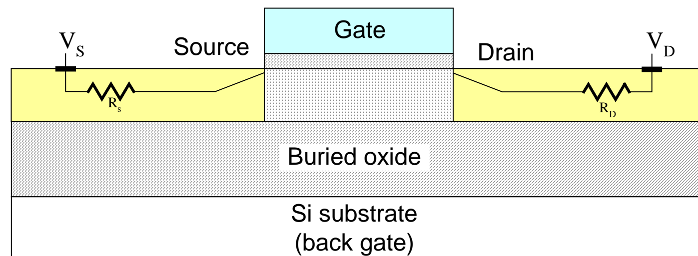

Shallow trench isolation; A: lithography and nitride/pad oxide/silicon etch; B: growth of sidewall thermal oxide, C:CVD oxide deposition and CMP; D: nitride and pad oxide strip.




Silicon island bending caused by oxide liner growth → lower surface mobility for electrons

H. Shang, M.H. White, D.A. Adams, Proceedings of the IEEE International SOI Conference, p. 37, 2002

## Source and drain resistance




- S&D resistance become important as silicon film thickness is reduced.
- Solutions: elevated S&D
  full or partial S&D silicidation
  metal (Schottky) S&D

Ref: 41-43

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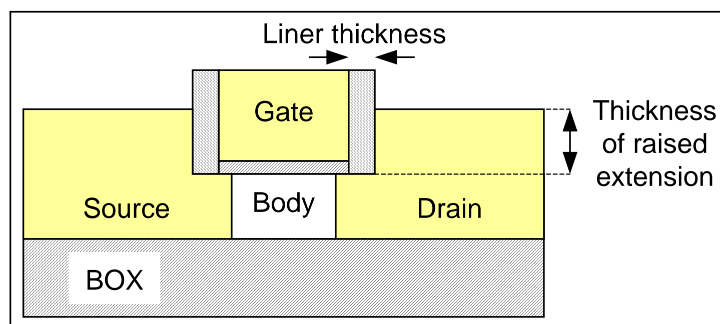
## Elevated source and drain





A. Vandooren, A. Barr, L. Mathew, T.R. White, S. Egley, D. Pham, M. Zavala, S. Samavedam, J. Schaeffer, J. Conner, B.Y. Nguyen, B.E. White, Jr., M.K. Orlowski, J. Mogab, IEEE Electron Device Letters, Vol. 24, no. 5, p. 342, 2003
S.S. Kim, T.H. Choe, H.S. Rhee, G.J. Bae, K.W. Lee, N.I. Lee, K. Fujihara, H.K. Kang, J.T. Moon, Proceedings of the IEEE International SOI Conference, p. 74, 2000
J.L. Egley, A. Vandooren, B. Winstead, E. Verret, B. White, B.Y. Nguyen, Electrochemical Society Proceedings, Vol. 2003-05, p. 307, 2003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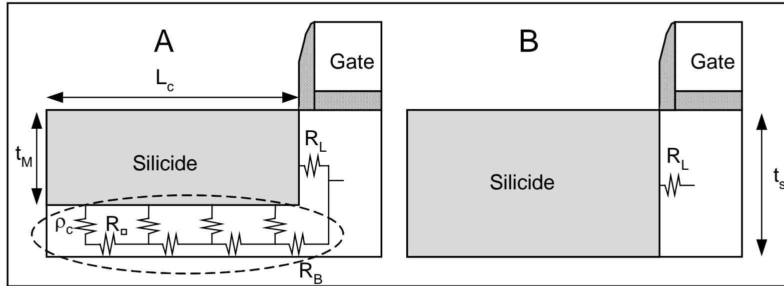
## Silicided source and drain




Current flow path in a silicide junction. A: the silicide is thinner than the silicon film; B: the silicide reaches the BOX


H.I. Liu, J.A. Burns, C.L. Keast, P.W. Wyatt, IEEE Transactions on Electron Devices, Vol. 45, no. 5, p. 1099, 1998
T. Ichimori, N. Hirashita, 2000 IEEE International SOI Conference. Proceedings, p. 72, 2000
T. Ichimori, N. Hirashita, Japanese Journal of Applied Physics Part 1, Vol. 40, no. 4B, p. 2881, 2001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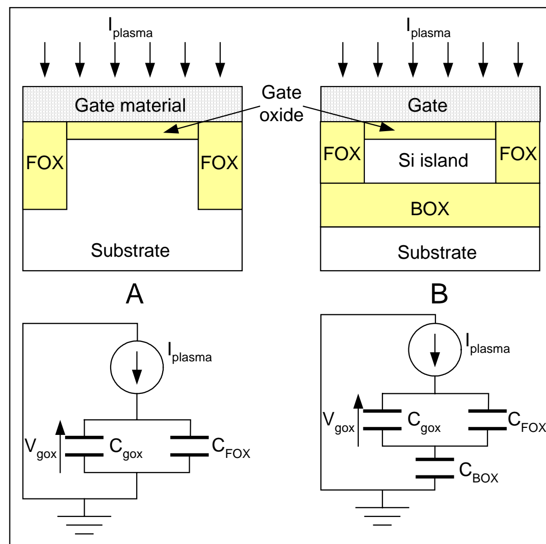
## Reduced antenna effect




Antenna effect during plasma etch step in bulk (A) and SOI (B)


A.O. Adan, T. Naka, A. Kagisawa, H. Shimizu, Proceedings of the IEEE International SOI Conference, p. 9, 1998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Several books have been published on SOI
Silicon-on-Insulator Technology: Materials to VLSI
Jean-Pierre Colinge
Kluwer Academic Publishers
SOI技术
21世纪的硅集成电路技术
微电子学系列
SOI
CIRCUIT DESIGN CONCEPTS
Kerry Bernstein
Norman J. Rohrer
Kluwer Academic Publishers
CMOS VLSI Engineering
Silicon-on-Insulator (SOI)
James B. Kuo and Ker-Wei Su
SILICON-ON-INSULATOR TECHNOLOGY:
Materials to VLSI, 2nd Edition
Jean-Pierre Colinge
KLUWER ACADEMIC PUBLISHERS
SILICON-ON-INSULATOR TECHNOLOGY:
Materials to VLSI, 3rd Edition
Jean-Pierre Colinge
KLUWER ACADEMIC PUBLISHERS
Electrical Characterization of Silicon-On-Insulator Materials and Devices
Sorin Cristoloveanu
Sheng S. Li
Kluwer Academic Publishers
SOI Design:
Analog, Memory and Digital Techniques
Andrew Marshall
Sreedhar Natarajan
Kluwer Academic Publishers