

# **New Devices to Extend Scaling of Non-volatile Memory**

Zoran Krivokapič  
Strategic Technology Group

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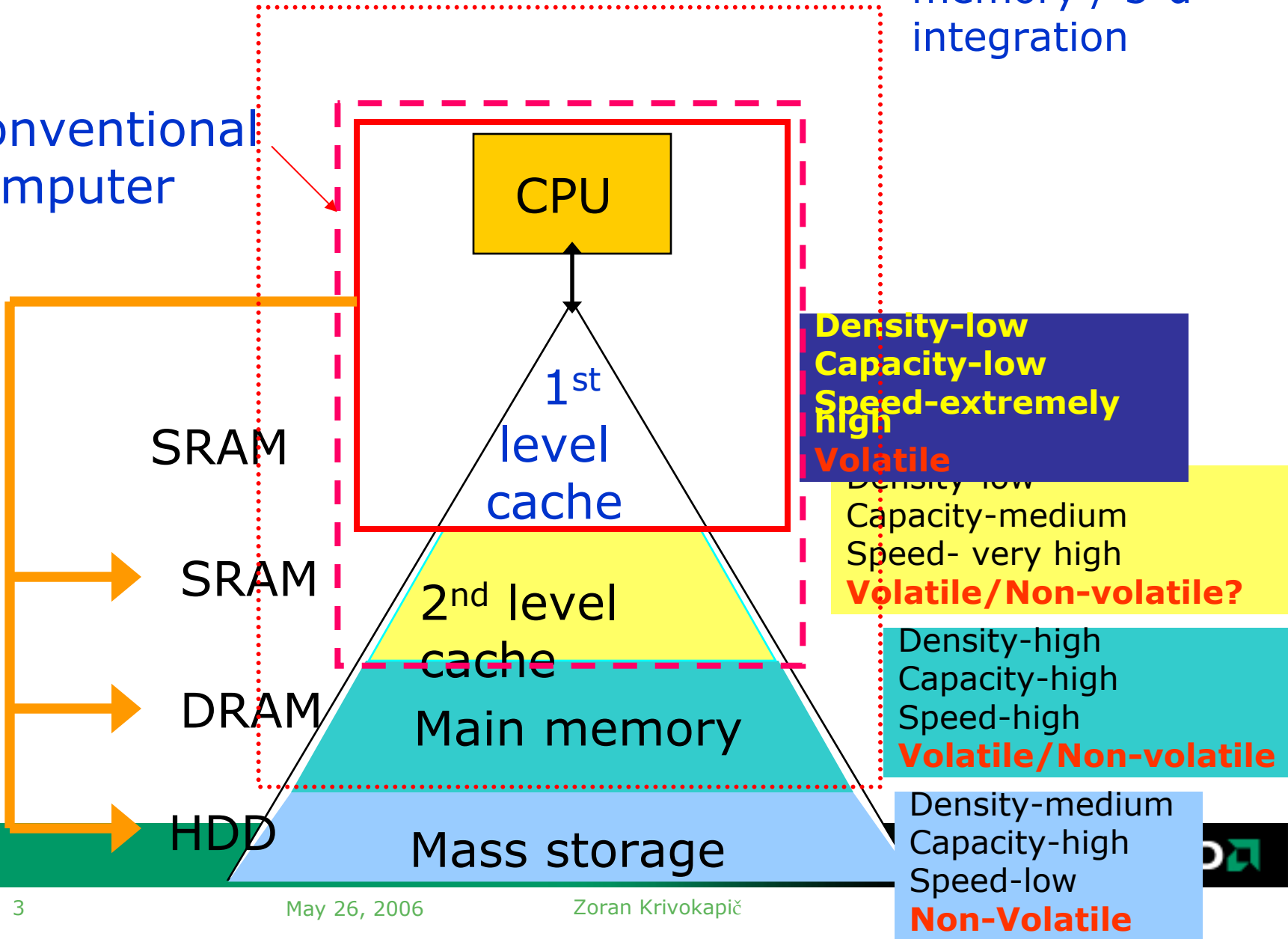
# Non-volatile Memory Outlook

- Scaling of non-volatile memories will become extremely difficult beyond the 32nm technology node.
- Higher level of integration requires larger amount of embedded memory. Since its performance cannot lag behind the logic it has become more challenging to realize a stable such a memory beyond the 45nm node.
- Conventional hard disk drive are being challenged by NAND devices and NEMS probe-storage devices.
- Large memory capacity can be achieved by 3-d integration and stacking layers of memory devices. To achieve that a BEOL-friendly selection device is needed.

# Memory Hierarchy

stackable  
memory / 3-d  
integration

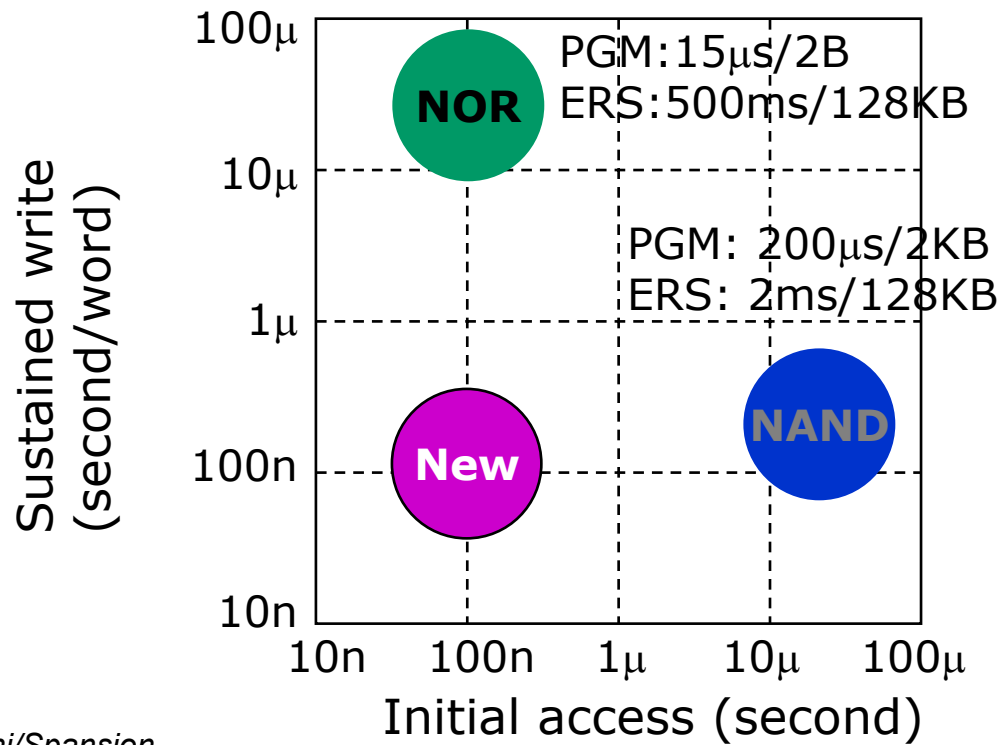
Conventional  
computer



# Current Outlook for Non-volatile Memory

- Conventional non-volatile memory is facing scaling difficulties. Code-storage NOR architecture may face challenge to extend beyond the 45/32nm node. Data-storage NAND architecture is better scalable and could reach beyond the 32nm node.
- Among established alternative/niche non-volatile memories PCM seems scalable beyond the 32nm node but is costly. MRAM will remain a niche memory with some improvements coming from exploiting spin torque, MgO tunneling layer or architecture based on anisotropic magnetization.

# Quest for New Non-volatile Memory



Slide from M.Taguchi/Spansion

# Scaling of Flash Memory

- Every aspect of scaling is detrimental for flash devices. Reducing the size of bit lines increases resistance, while shortening the channel length worsens the short channel effect.
- The problem is in the trade-offs between writing speed and data retention. To guarantee a ten year data retention one cannot thin down the tunneling dielectric of conventional flash devices.
- In order to alleviate this problem barrier engineering has been proposed using new devices and new materials.

# How to Improve Scaling?

Direct tunneling current, *Lee&Hu, VLSI Symp. 2000*)

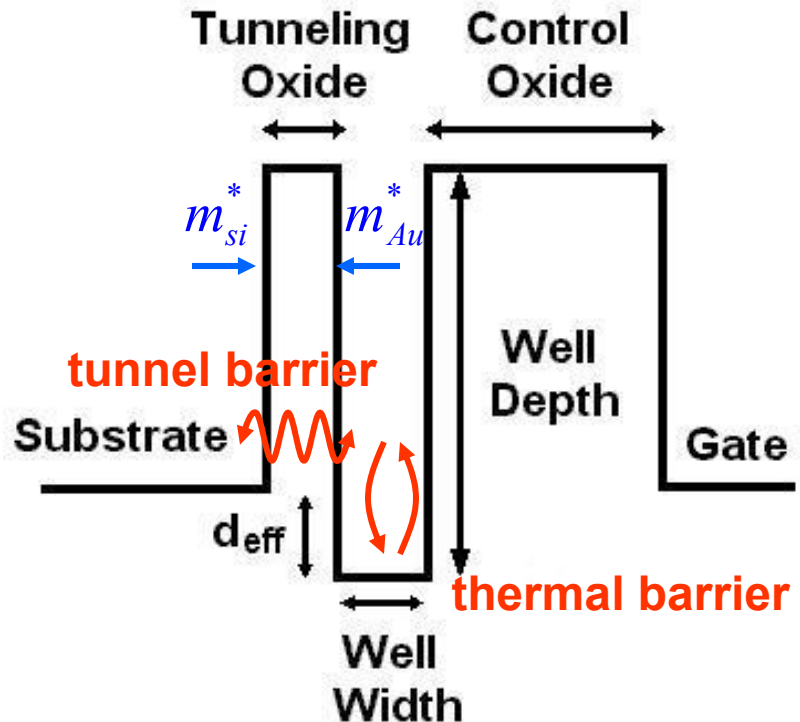
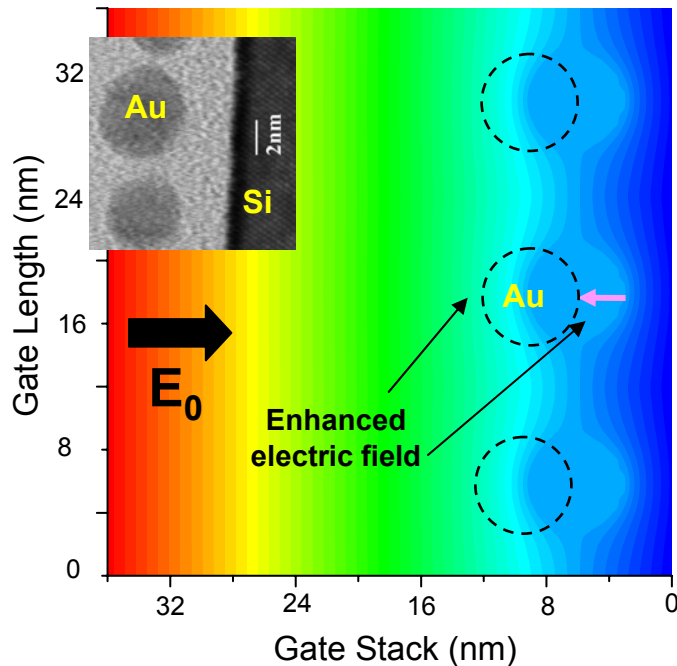
$$J_n = \frac{q^3}{8\pi\hbar\phi_b\epsilon_{ox}} f(V_g, V_{ox}, T_{ox}, \phi_b) \exp\left(-\frac{8\pi\sqrt{2m_{ox}}\phi_b^{1.5}\left(1-\left(1-\frac{|V_{ox}|}{\phi_b}\right)^{1.5}\right)}{3hq|E_{ox}|}\right)$$

There are three material parameters we can play with to improve speed/retention trade-off (*E. Kan/Cornell*):

- 1) Difference in barrier height for retention and injection
- 2) Electric field asymmetry
- 3) Difference in tunneling effective masses for retention and injection

# Metal Nanocrystals

- **Asymmetric electrostatic field enhancement** between write (from control gate bias) and retention (from stored charge)
- **Work function engineering:** two energy barriers (large work function metal) to achieve  $t_{ret}/t_{wr} > 10^{16}$ .
- **Effective mass engineering:** asymmetric nonequil. injection
- **Higher density of states:** more stable Fermi level



# Plethora of Other Candidates

There are significant research efforts underway to find a replacement for non-volatile, DRAM, and SRAM memory based on new phenomena in less CMOS-common materials like:

- Complex metal oxides
- Correlated electron systems
- Solid electrolytes
- Molecular devices
- Polymer devices
- CNT

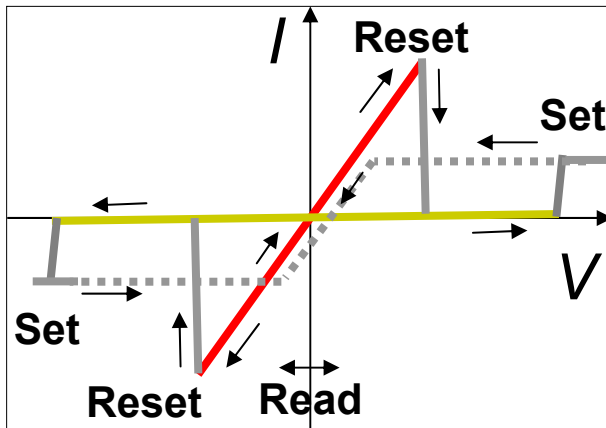
Table 27 Emerging Research Memory Devices—Demonstrated and Projected Parameters

		Non-floating Gate Memory [A]	Engineered Tunnel Barrier Memory	Ferroelectric FET Memory	Insulator Resistance Change Memory	Polymer Memory	Molecular Memory
Storage Mechanism		Charge on floating gate	Charge on floating gate	Resonant polarization on a ferroelectric gate dielectric	Multiple mechanisms	Not known	Not known
Cell Elements		1T	1T	1T	1T1R or 1R	1T1R or 1R	1T1R or 1R
Device Type		1 Nanocrystal 2-Direct tunneling	Graded insulator	FET with FE gate insulator	1 M-1-M 2 Solid Electrolyte 1 FE tunneling 4 FE Solvolytic diode 3 FE-1-SE	M-1-M (no)-1-M	Bi-stable switch
Feature size <i>F</i>	Minimum required	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm
	Best projected	25 nm	10 nm [H]	22 nm [K]	5–10 nm [O]	5–10 nm	3–10 nm [AA]
	Demonstrated	60 nm [A]	100 nm [I]	~10 nm [L]	100 nm [F]	200 nm [W]	10 nm [AD]
Cell Area	Minimum required	10 <sup>4</sup>	10 <sup>2</sup>	10 <sup>2</sup>	10 <sup>4</sup>	10 <sup>4</sup>	10 <sup>4</sup>
	Best projected	0–10 <sup>2</sup>	10 <sup>2</sup> [H]	10 <sup>2</sup>	0–10 <sup>2</sup> [O]	10 <sup>2</sup>	10 <sup>2</sup>
	Demonstrated	10 <sup>2</sup> [A]	Data not available	Data not available	Data not available	Data not available	Data not available
Read Time	Minimum required	<15 ns	<15 ns	<15 ns	<15 ns	<15 ns	<15 ns
	Best projected	2.5 ns	2.5 ns	2.5 ns	<10 ns	<10 ns	<10 ns [AA]
	Demonstrated	20 ns [D]	20 ns [D]	20 ns [D]	2 ns [E]	~10 ns [X]	Data not available
Write Time	Minimum required	1 μs/10 ns	1 μs/10 ns	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	1 μs/10 ns	1 ns at 1V [H]	2.5 ns [D]	<20 ns [E]	Not known	<10 ns [AA]
	Demonstrated	W: 1–10 μs [C] R: 10–100 ns [C]	R: ~10 ns [I]	100 ns [L]	25 ns [F]	<10 ns [X]	~ns [AC]
Retention Time	Minimum required	>10y	>10y	>10y	>10y	>10y	>10y
	Best projected	>10y	>10y	>1y	>10y	Not known	Not known
	Demonstrated	>100 hours [B]	>10y [I]	30 days [H]	1y [E]	6 months [Y]	2 months [AC]
Write Current	Minimum required	>10S	>10S	>10S	>10S	>10S	>10S
	Best projected	>10S	>10E6	>10E6	>10E6	>10E6	>10E6
	Demonstrated	>10E [A]	10E [Z]	10E2 [O]	10E [T]	>10E [X]	>10E [AD]
Write Operating Voltage (V)	Minimum required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	>1 V [F]	>1 V [F]	<0.5 V [K]	<0.5 V [L]	Not known	2 V [AG]
	Demonstrated	1E [A]	4.5 [Z]	1E [O]	0.24 V [E]	~1E [X]	~1.5 V [AD]
Read Operating Voltage (V)	Min. required	2.5	2.5	2.5	2.5	2.5	2.5
	Best projected	0.7	0.7	0.7	<0.5 V [L]	0.7	0.5 [AA]
	Demonstrated	2.5 [D]	2.5 [D]	2.5 [D]	<0.2 V [F]	~1 [X]	0.5 [AD]
Write Energy (fJ/cy)	Min. required	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent	Application dependent
	Best projected	1E–1E [Z]	1E–1E [Z]	1E–1E [O]	1E–1E [V]	Not known	1E–1E [AA]
	Demonstrated	1E–1E [Z]	Data not available	Data not available	1E–1E [F]	1E–1E [X]	Data not available
Comments		A, natural evolution of the floating gate memory		Potential for non-destructive readout	Low read voltage presents a problem		

# Resistive RAM Memories

## Unipolar/Symmetric Switching

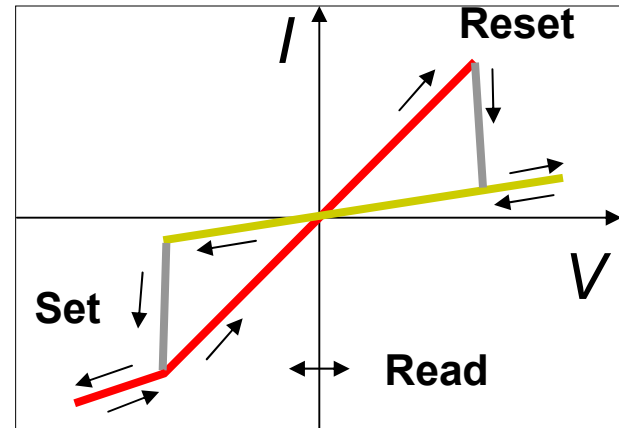
R/W/E require only positive bias of cell



Example: phase change memory

## Bipolar /Asymmetrical Switching

W/E require opposite polarity



Example: Axon metallization cell

# Complex Metal Oxides

Various M-I-M structures with insulator being NiO, CuO<sub>x</sub>, Nb<sub>2</sub>O<sub>5</sub>, Ta<sub>2</sub>O<sub>5</sub>, VO<sub>2</sub>, TiO<sub>2</sub>, STO, PZTO, PCMO etc. showed memory effects.

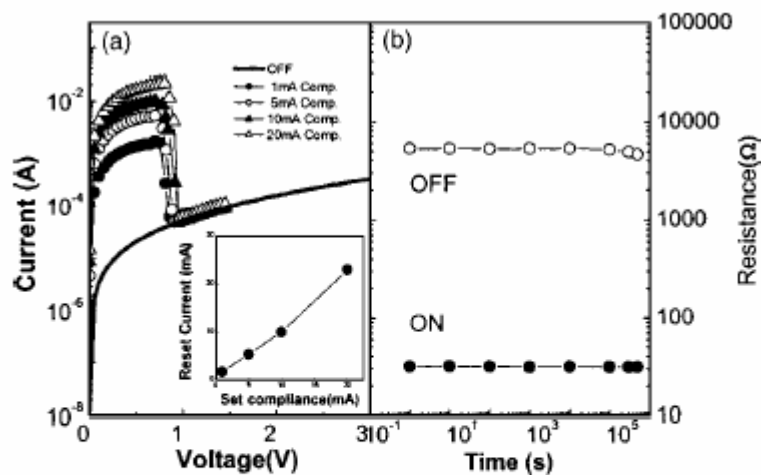
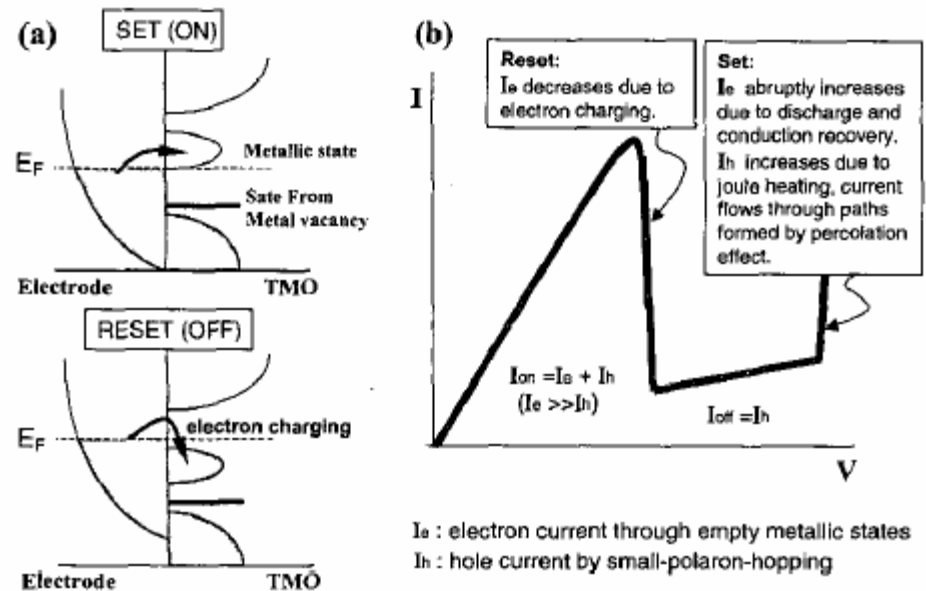


FIG. 3. (a) Conduction switching behaviors of a NiO film deposited at 5% oxygen content under different magnitudes of the compliance current from 1 to 20 mA; The inset shows the linear relation between ON state current and the compliance SET current. (b) Retained resistance values of a NiO film at 5% oxygen content showing bi-stable memory switching at 200 °C for  $5 \times 10^5$  s.



$I_e$  : electron current through empty metallic states  
 $I_h$  : hole current by small-polaron-hopping

*I.G. Baek et al, IEDM 2004, p.587*

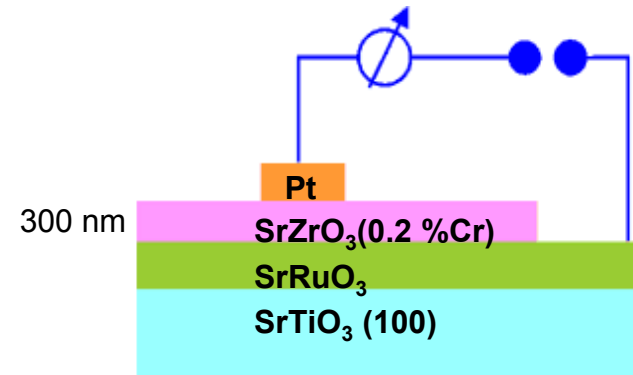
Physical mechanism not fully known, understanding of endurance and retention in infancy.

*From S. Seo et al, APL, 85, p.5655, Dec. 2004*



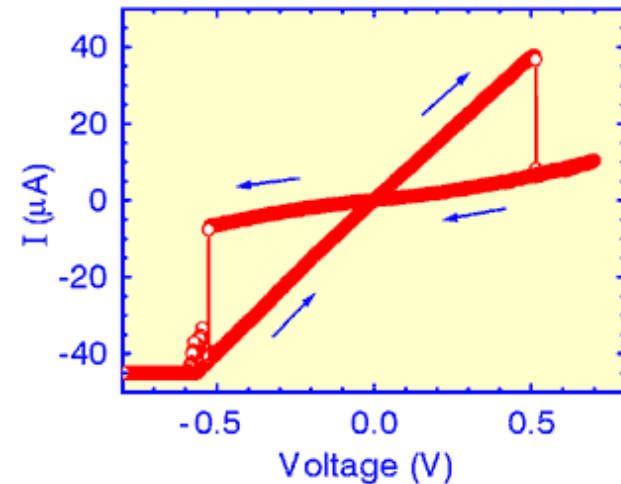
# Redox-based Resistive Switching

- Capacitor-like structure with
- ▶ Cr-doped  $\text{SrZrO}_3$  thin films
  - ▶  $(\text{Ba},\text{Sr})\text{TiO}_3$  thin films
  - ▶  $\text{SrTiO}_3$  Single crystals as resistive element



## Characteristics

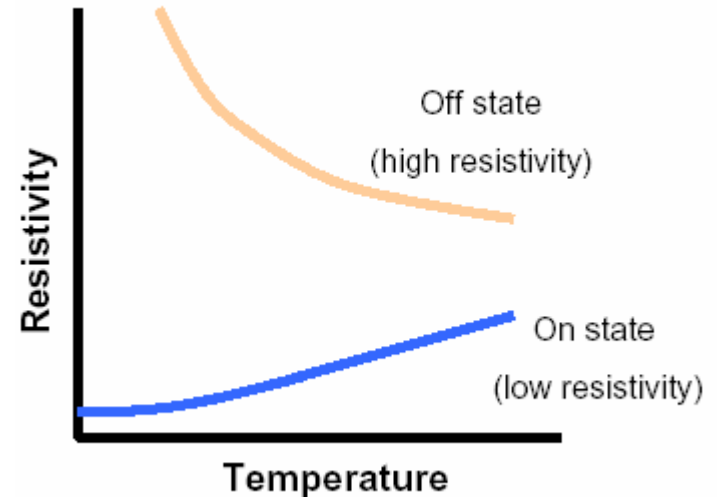
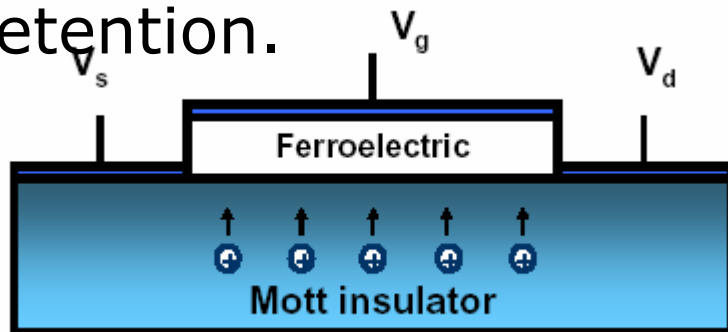
- **after forming process: reversible switching between stable impedance states**
- **non-volatile**
- **non-destructive read-out**
- **multilevel memory**



# Correlated Oxides

Crystalline ferroelectric film induces large inversion charge in the Mott insulator.

Demonstrated memory uses low  $V_g$  ( $<1V$ ), has excellent endurance and retention.



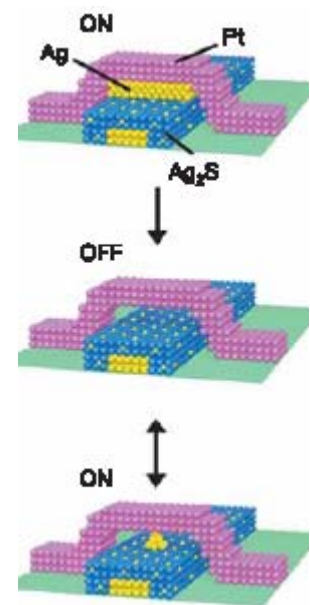
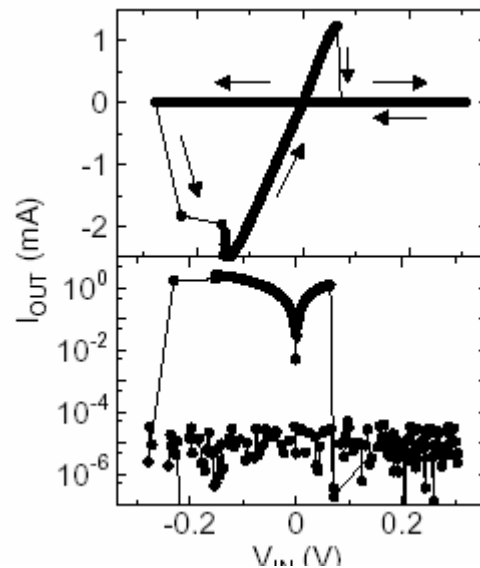
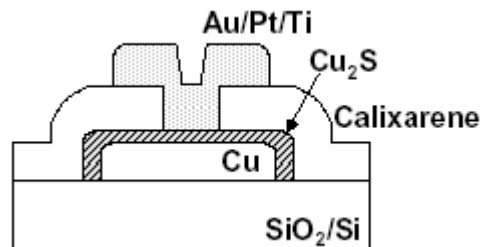
Demonstrated  $I_{on}/I_{off}$  ratio of 3 at room temperature for a low Sr concentration in LSMO. The ratio will increase with more chemical doping of Sr.

# Solid Electrolytes

Solid electrolytes ( $\text{Cu}_2\text{S}$ ,  $\text{Ag}_2\text{S}$ ) show memory effect that is caused by ion conduction.

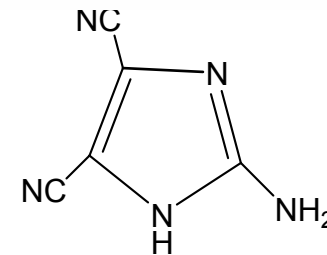
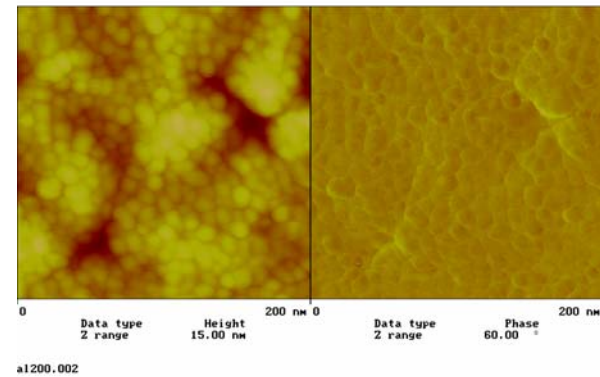
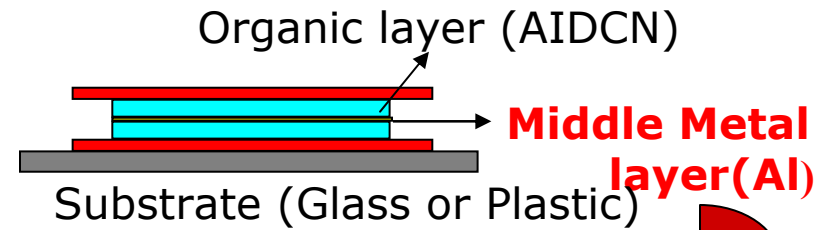
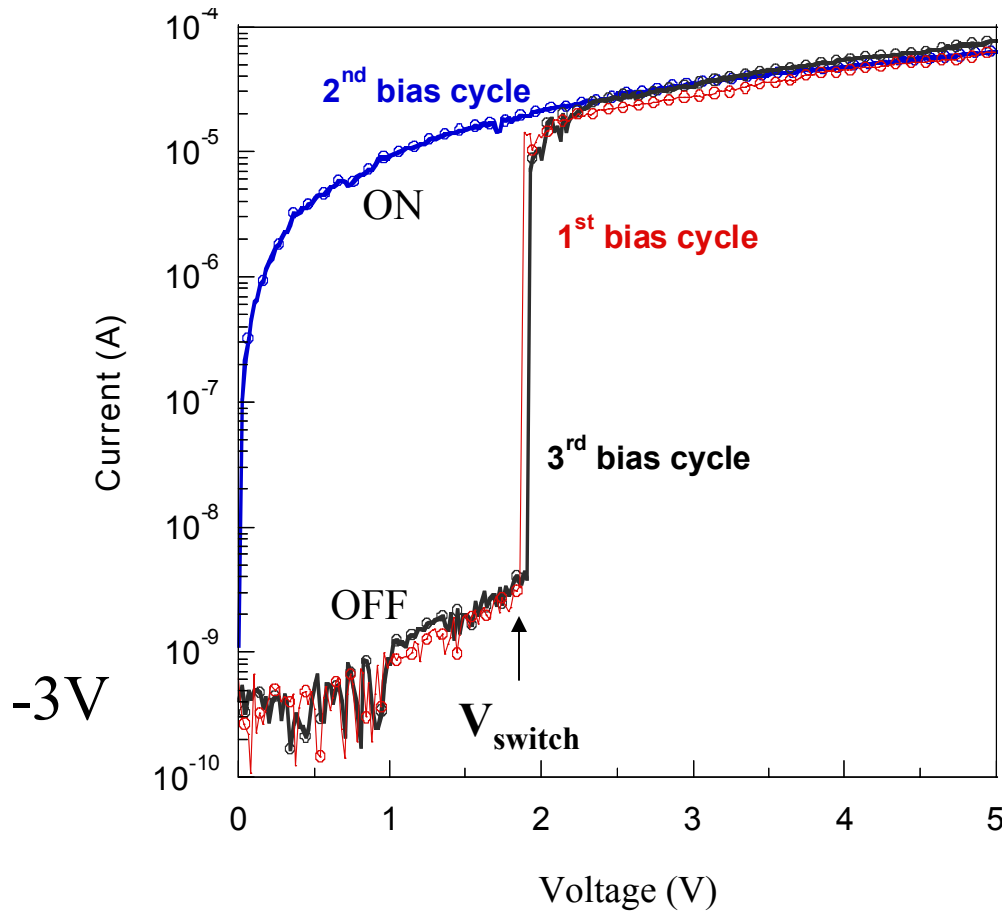
Advantages: small voltage, small cell size.

Disadvantage: retention.



*K. Terabe et al, Nature, 433, p.47, Jan. 2005*

# Polymer Memory



2-amino-4,5-imidazole dicarbonitril (AIDCN)

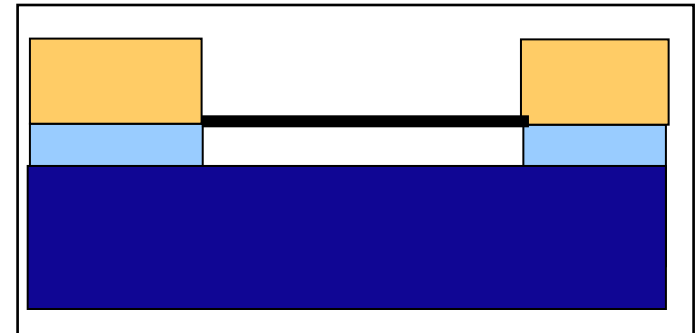
# CNT-based Non-volatile Memory

Memory exploits two stable states formed by interaction of mechanical strain and Wan der Walls force.

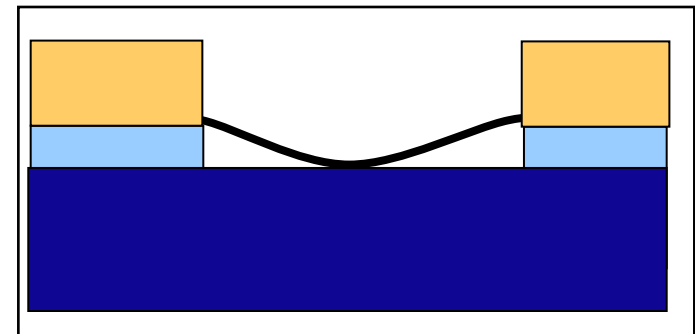
Memory is non-volatile with infinite endurance, fast and small.

More sophisticated memory devices are possible if strain effect on CNT band-gap is exploited.

OFF State

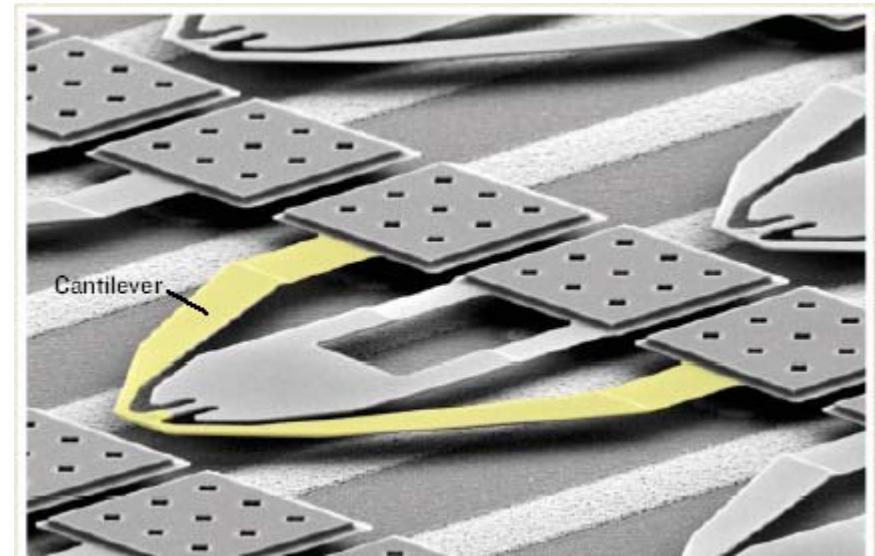


ON State



# Probe-Storage Devices

There is significant interest in replacing less reliable HDD with other mass storage devices. One of the potential candidates is a NEMS-based probe-storage memory.



Write: press a heated ( $400^{\circ}\text{C}$ ) tip into polymer

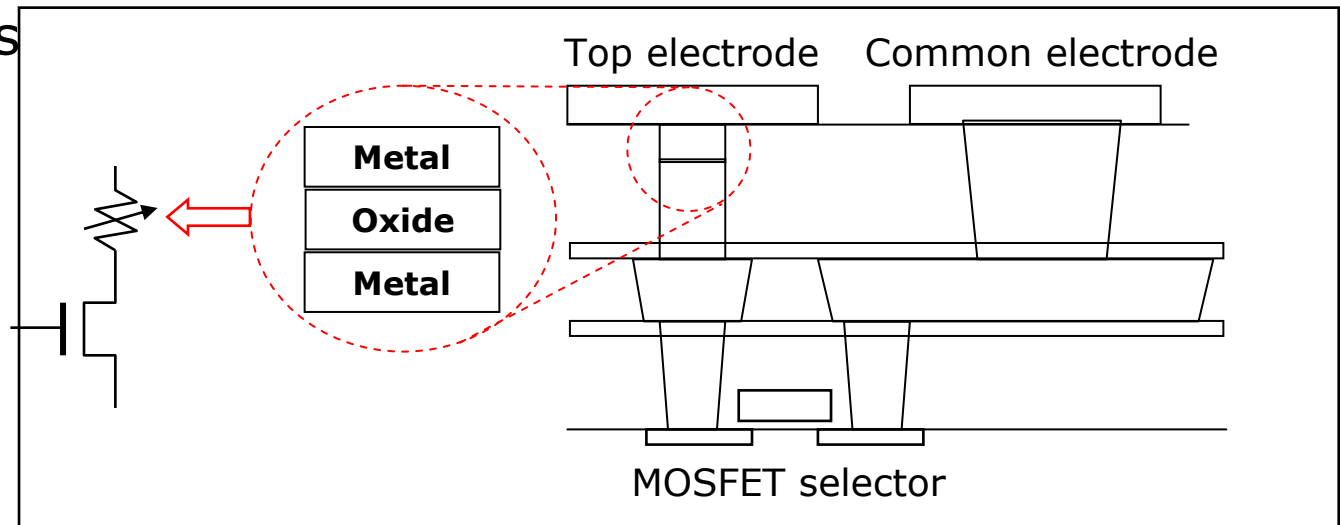
Read: polymer cools down a heated ( $200^{\circ}\text{C}$ ) tip, changing resistance

Erase: press an adjacent hole flattening the original one



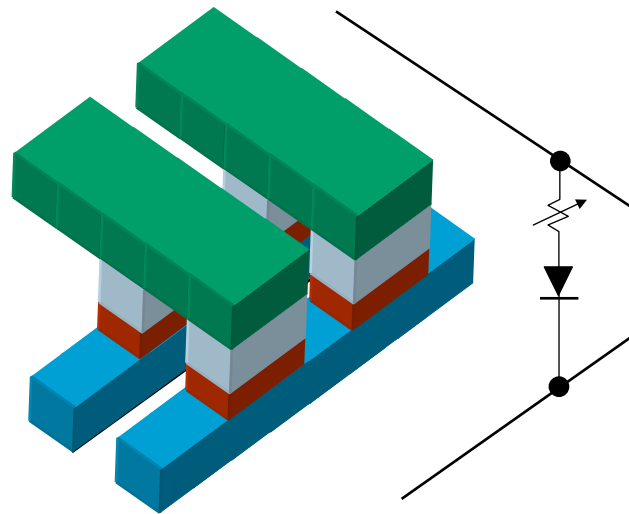
## Three-terminal Selection Device

- MOSFET selector type
  - $6F^2$  cell
  - No need for strictly low leakage transistors
    - Potential advantage for bidirectional devices
    - Selection is more conventional (similar to DRAM).
- Material engineering
  - Switching element
  - Electrodes



# Two-terminal Selection Device

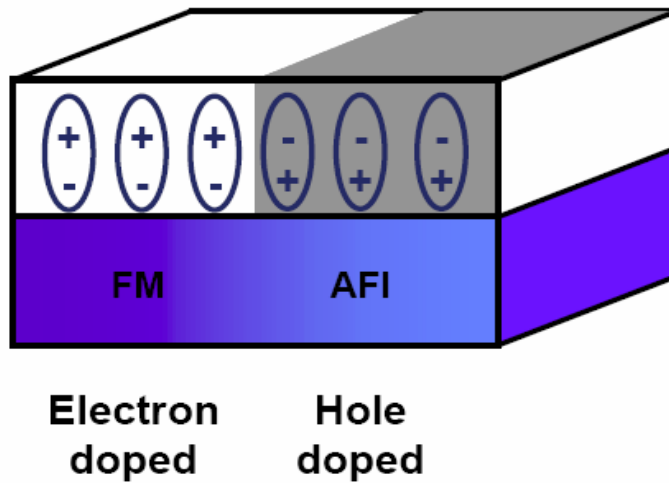
- Thin-film diode selector type
  - 4F<sup>2</sup> cell
  - Multi-layer stackable
- No scaling limitations by diode + memory element
- Material engineering (Low-T BEOL processing)
- Architectural engineering and control logic



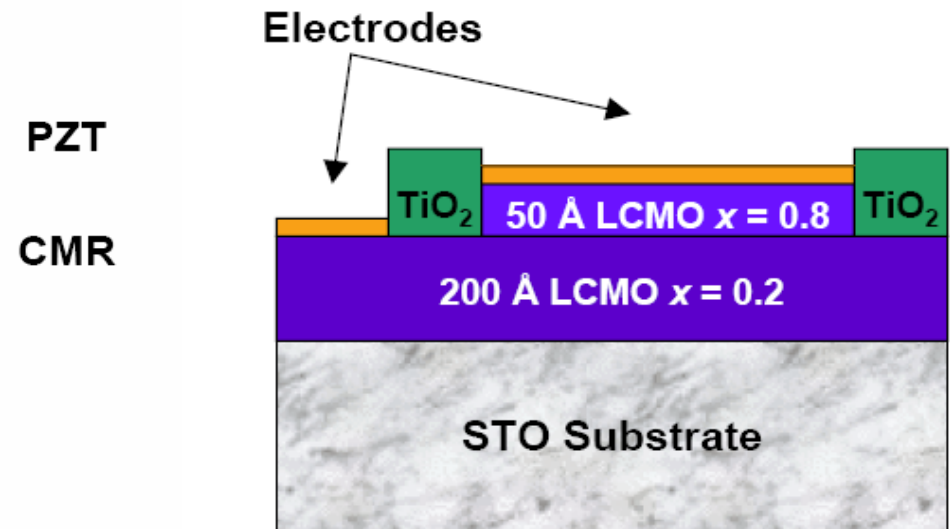
- ❖ Unipolar memories require low forward  $R_{on}$  and low reverse leakage and high reverse breakdown voltage.
  - ❖ Bidirectional devices add requirements for reverse BV
- Selection requires careful biasing of unselected rows and

# LCMO-based Back-end Diode

- Lateral Junction



- Vertical Junction



# Material and Device Challenges

- There is no obvious winner in replacing conventional non-volatile memory
- New candidates require materials that are new to semiconductor manufacturing
- Operation of some candidates is not well understood and engineering them into a solid product can be challenging
- 3-d integration requires a BEOL-type selection device that is very challenging